1. INTRODUCTION

This application note is designed to assist the Fairchild F8 Microprocessor family user in the real time analysis of his system in both design and troubleshooting environments. The note demonstrates real time analysis of actual program sequences, triggering on specific events, selective data qualification, and paging techniques.

The Microprocessor and Read Only Memory form a basic two chip system that will handle most simple tasks. For more complex processing functions the memory access and interface chips complete a four chip set. The F8 System is unique in that each chip has its own resident program counter eliminating the need for a dedicated address bus and its associated circuits. Branch commands which require resetting the address counter are multiplexed onto the data bus for implementation. This architecture makes possible a very low cost system including I/O ports as a standard part of the basic chips.

2. PIN ASSIGNMENTS

Central Processing Unit Chip Pin Assignments

<table>
<thead>
<tr>
<th>PIN NAMES</th>
<th>DESCRIPTION</th>
<th>TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB 0 - DB 7</td>
<td>Data Bus</td>
<td>Bidirectional</td>
</tr>
<tr>
<td>I/O 00 - I/O 07</td>
<td>I/O Port Zero</td>
<td>Input/Output</td>
</tr>
<tr>
<td>I/O 10 - I/O 17</td>
<td>I/O Port One</td>
<td>Input/Output</td>
</tr>
<tr>
<td>ROMC 0 - ROMC 4</td>
<td>Control Lines</td>
<td>Output</td>
</tr>
<tr>
<td>RC</td>
<td>RC Timing Input</td>
<td>Input</td>
</tr>
<tr>
<td>XTL-X</td>
<td>Crystal Clock Inputs</td>
<td>Input</td>
</tr>
<tr>
<td>XTL-Y</td>
<td>External Clock Inputs</td>
<td>Input</td>
</tr>
<tr>
<td>EXT RES</td>
<td>External Reset</td>
<td>Input</td>
</tr>
<tr>
<td>Φ_WRITE</td>
<td>Clocks</td>
<td>Output</td>
</tr>
<tr>
<td>IC</td>
<td>Interrupt Control Bit</td>
<td>Output</td>
</tr>
<tr>
<td>INT REQ</td>
<td>Interrupt Request</td>
<td>Input</td>
</tr>
<tr>
<td>VDD, VSS, VGG</td>
<td>Power</td>
<td>Input</td>
</tr>
</tbody>
</table>
4. SETTING THE CONTROLS

Turn power on and set the Logic State Analyzer Controls as follows:

- Display Mode - Table A
- Sample Mode - REPET
- Start Display - ON
- Trigger Mode - NORM
  - LOCAL
  - WORD
- Threshold - TTL
- Clock slope -
- All other pushbuttons - out
- Display Time - ccw
- Column Blanking - ccw
- Qualifiers - Q0-HI, Q1-OFF
- Trigger Word switches - Set to Address at which you wish to trigger*

*If program is not looping or cycling through the selected address, select "Single", press "Reset" and start your system. The first time the system passes through the selected trigger state the display will be generated and stored.

5. DISPLAY INTERPRETATION

Figure 1 illustrates a portion of a start-up program to help you understand the Logic State Analyzer display. Your program will work equally well. Proper operation is confirmed by a comparison between real time state analysis and the start-up program.

With Q0 probe connected to CPU READ, Q0 set HI, and triggering on address 0000, an address is incremented with every memory fetch. Notice that the address sequence branches after address 000D where it loops back to clear all F8 scratch pad registers, and then the program is re-entered at address 000E.

It is easy to determine whether this loop is completed by using the "Paging" technique. Reset the Logic State Analyzer trigger word switches to address 000D and restart the system. The display then begins at address 000D and the next 15 addresses are displayed.

Some addresses in the start-up program involve multiple word instructions. These may be observed on the display as redundant consecutive addresses by placing the Q0 switch in the OFF position.
6. THE MAP

If a tabular display is not presented in the previous step it means the system did not access the selected address and the No Trigger light will be on. To find where the system is residing in the program switch to "map" (figure 2). Using the Trigger Word switches move the cursor to encircle one of the dots on screen. Switch to expand and make the final positioning of the cursor---the No Trigger light will now go out and switching back to Table A displays the 16 bit address around that point.

By combining the 1600A and 1607A the display and trigger capability can be expanded to 32 bits wide, allowing the 16 bit address, 8 bit data bus, and eight other active command signals to be viewed simultaneously. A typical test setup is shown in figure 3. The hookup is easy.

7. VIEWING ADDRESS, DATA, AND CONTROLS

When program deviations are found, the reason may be as simple as a program error or as complicated as a hardware failure on the Data Bus, Control Bus, or other command lines. Additional input channels now become very desirable.
5. Select Threshold and Logic Polarity on 1607A to be the same as the 1600A.
6. Leave all other pushbuttons out.
7. 1600A data and clock inputs connected for address as described in Part 3.
8. Set Q0 and Q1 off.
9. Connect data and clock inputs for 1607A to the MI as follows:
   a. 1607A Data inputs 0 through 7 to DB 0 through DB 7 in order.
   b. 1607A Data Input 8 to pin 34 CPU READ.
   c. Q0 to pin 34, CPU READ.
   d. Clock to pin 3.
   e. Grounds to appropriate point(s).
10. Set Column Blankings to display 9 columns on the 1607A.

8. DISPLAY INTERPRETATION OF ADDRESS AND DATA BUSINES AND CPU READ CONTROL LINE

As an amplification of the previous example, it is possible to investigate all the activity on the address and data buses plus the CPU READ control line.

Operating the Logic State Analyzer system as set up in section seven, the display shows all activity on the address bus as well as on the data bus during the start-up program. In addition, the CPU READ control line is monitored to permit confirmation of system performance.

Figure 4 illustrates multiple-word instruction addresses and at the same time shows activity on the address bus during the execution of the instruction. At address 0004, the data bus indicates that I/O Port 08 is addressed. Then, contents of the accumulator are sent to the I/O Port. In the next instruction, CPU READ is high and the data bus shows that the instruction has been completed at instruction code B9 and the program counter has been incremented to the next address. In a similar manner, each address in the program may be analyzed.

9. CONCLUSION

From the foregoing examples it may be concluded that efficient troubleshooting of the Fairchild F8 Microcomputer System is expedited by two factors; FIRST: the availability of the program listing as produced by F8 cross assembler, which is the definitive document of program execution and; SECOND: the availability of real time Logic State Analysis to display actual system operation for rapid error detection and correction.