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APPLICATION NOTE 912

AN ATTENUATOR DESIGN USING PIN DIODES

Constant Impedance

Current Controlled

10 MHz to 1.0 GHz Bandwidth

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Since its introduction, the PIN diode has found use in many unique applications. This article describes its use as an element in a constant impedance current controlled attenuator.

Such an attenuator can be used as a remote, programmable or automatic gain control element in circuits where a minimum effect on the source and load is required. It is particularly useful as an interstage gain control element in transistor amplifiers where it will provide a wide range of gain control without disturbing the optimum operating bias point of the transistors. This minimizes changes in transistor input and output impedance levels, phase shift, and tuning while achieving the required change in overall gain.

The PIN diode used in this attenuator is distinguished from a normal p-n type junction in that it has an intrinsic region sandwiched between the p^+-doped and the n^+-doped silicon layers. This intrinsic region has almost negligible doping; and consequently a very high resistance. This high resistance and a relatively large I-layer width result in extremely low junction capacitance and high breakdown voltage. When forward bias is applied across the diode, the conductivity of the I-layer is increased by the injection of minority carriers into the I-layer. If the diode's minority carrier lifetime is adjusted so that it is relatively long (typically greater than 100 ns) then it is found that high frequency currents see the diode as essentially a resistance. This RF resistance is controllable by adjusting the forward bias on the diode. The lowest frequency of operation is determined by the minority carrier lifetime and for lifetimes around 100 ns it is typically 10 MHz.

For frequencies much below 10 MHz, the PIN diode appears as a standard rectifier diode. Partial rectification will also be observed near the low frequency limits if the peak level of the RF signal is of a sufficient magnitude on reverse bias half cycles to deplete the minority carriers in the I-layer.

The following may be considered as the equivalent circuit at radio frequencies above 10 MHz:

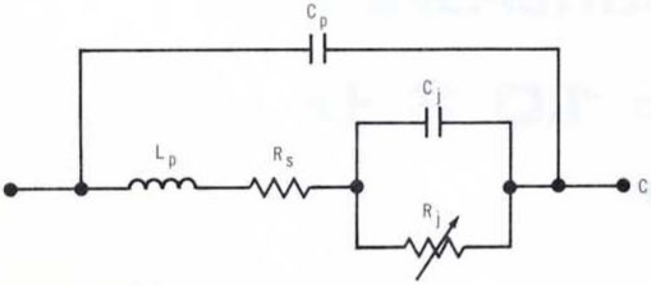


Figure 1

	3001 3002	3101 3102	3201 3202
Where C_p = package capacitance (typical value)	0.18 pF	0.20 pF	0.20 pF
C_j = junction capacitance (typical value)	0.07 pF	0.07 pF	0.07 pF
L_p = package inductance (typical value)	3 nH	0.5 nH	0.4 nH
R_s = parasitic series resistance (typical value)	2.5 Ω	2.5 Ω	2.5 Ω
R_j = conductivity modulated junction resistance	—	—	—

Under the forward bias the intrinsic layer resistance varies according to the following relationship:

$$R_i = 26\,I^{-0.87} \qquad (1)$$

where I is the forward bias current in ma.

This relationship is good for the range of bias current between 10 μA and 10 mA. Above 10 mA the parasitic series resistance of approximately 2.5 Ω is approached and towards zero bias and reverse bias a limit of 10,000 Ω is asymptotically approached. This variation of resistance is shown in Figure 2. It is this characteristic of the PIN diode that makes it ideally suitable for use in a voltage controlled attenuator.

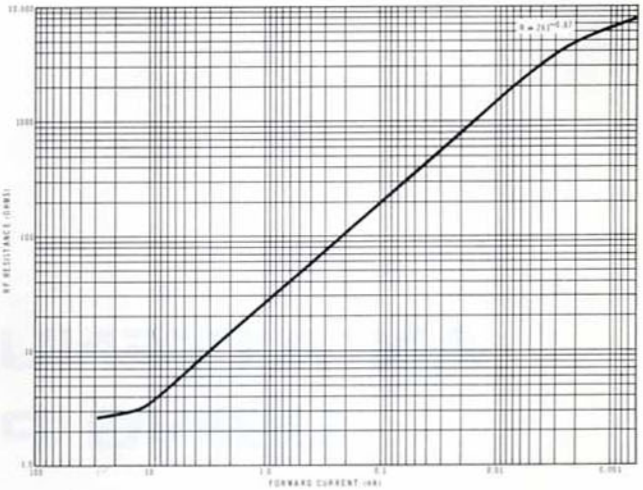


Figure 2

DESIGN OF CONSTANT IMPEDANCE ATTENUATOR

A constant impedance attenuator can be achieved by a proper selection of resistance values for the symmetrical π-network consisting of R_1 and R_3 shown in Figure 3.

Let the impedance of the network to the right of AA′ be indicated as Z_A, where

$$Z_A = \left[R_3 + \frac{R_1 Z_0}{R_1 + Z_0}\right] \qquad (2)$$

For the matched condition the input impedance of the network must equal the source impedance.

Therefore:

$$\frac{1}{Z_0} = \frac{1}{R_1} + \frac{1}{Z_A} \quad \text{or } Z_A = \frac{R_1 Z_0}{R_1 - Z_0} \qquad (3)$$

$$E_1 = I_1 Z_A \quad \text{or } I_1 = \frac{E_1}{Z_A} \qquad (4)$$

$$E_2 = I_1\left[\frac{R_1 Z_0}{R_1 + Z_0}\right] \qquad (5)$$

$$\frac{E_1}{E_2} = \frac{Z_A}{\left[\dfrac{R_1 Z_0}{R_1 + Z_0}\right]} = \frac{\left[\dfrac{R_1 Z_0}{R_1 - Z_0}\right]}{\left[\dfrac{R_1 Z_0}{R_1 + Z_0}\right]} = \frac{R_1 + Z_0}{R_1 - Z_0} = K \qquad (6)$$

R_1 and R_3 can be expressed in terms of the characteristic impedance of the network (Z_o) and the input to output voltage ratio K as follows:

$$R_1 = Z_0\left[\frac{K+1}{K-1}\right] \qquad (7)$$

and from the initial equation:

$$R_3 = \frac{Z_0}{2}\left[K - \frac{1}{K}\right] \qquad (8)$$

From the above relationships we can plot the variation of the pi arm resistances with respect to the input-output

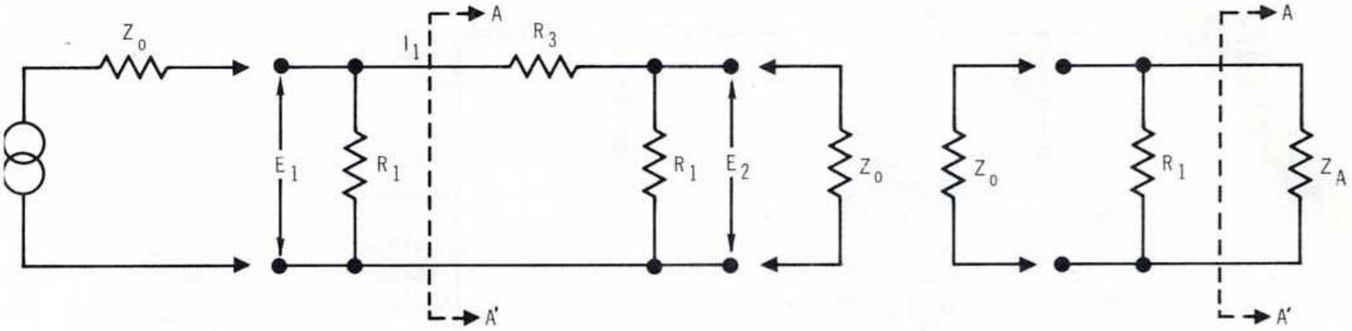


Figure 3

voltage ratio K. K may also be expressed as power attenuation in dB. These relationships are shown plotted in Figure 4 for the case of $Z_o = 50\ \Omega$.

Since the PIN diode has an RF resistance characteristic that is a function of bias as shown in Figure 2, it can be a suitable resistance element for use in such an attenuator. Using this curve as a transfer function, a plot of the attenuator's attenuation with respect to the bias currents needed to produce the necessary resistance values for R_1 and R_3 can be made. This is shown in Figure 5. All that remains is the design of a circuit that will suitably incorporate the PIN diodes in an RF transmission-type structure and which incorporates the necessary dc biasing circuitry for control of the PIN diode resistances. The design of such a structure with the following performance goals is described below:

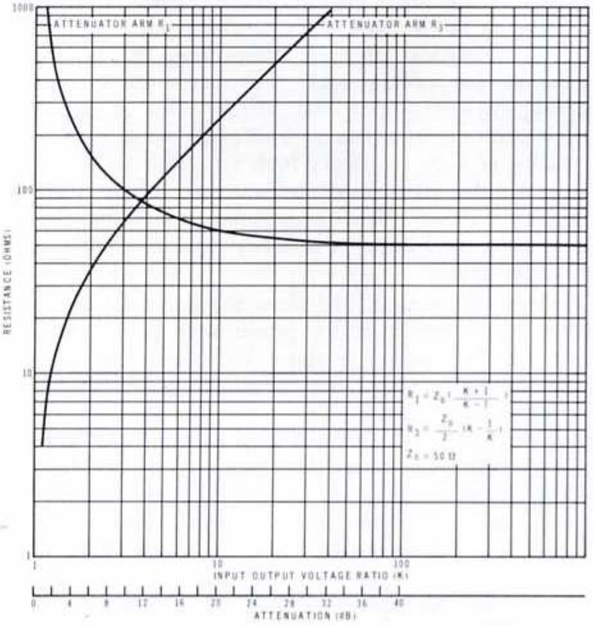


Figure 4

Frequency Range	10 MHz to 1 GHz
Attenuation Range	1 to 20 dB
VSWR	2:1 maximum over entire frequency range

It was found practical to achieve the necessary attenuation control using one variable current source and one constant voltage source. Since the range of frequency operation is quite wide, it was found that the parasitic reactances of the network had to be reduced to the lowest possible values to minimize phase shift and reflections. Microstrip techniques were used in conjunction with planar dielectric capacitors and pill packaged PIN diodes. Over narrower frequency ranges and at lower frequencies, conventional components and glass packaged diodes could be used just as well. Figure 6 shows the circuit used in the final attenuator layout.

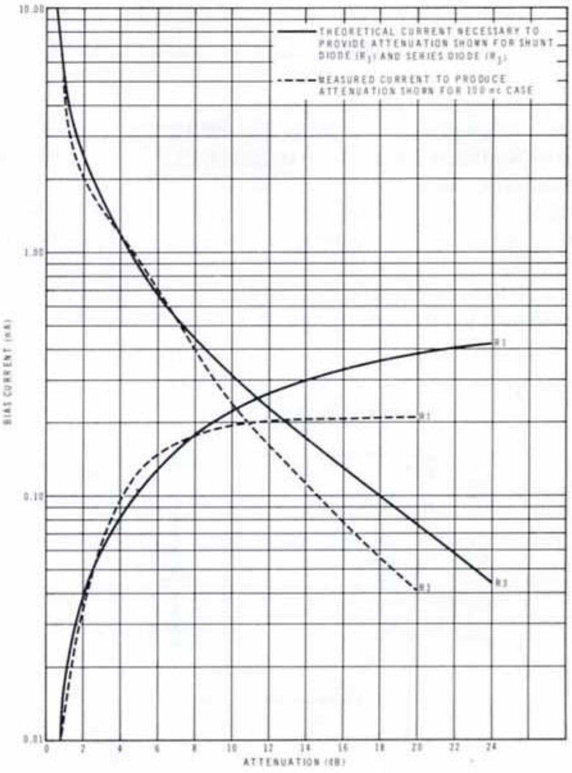


Figure 5

A variable bias current, which is supplied through a low pass filter, directly controls the resistance of R_3. This current also indirectly controls the resistance of R_1 by subtracting from the bias current that is supplied by the 9.0 V bias source. In this manner it is possible to produce the increasing dc current through the series arm simultaneously with a decreasing current through the shunt arms, as required by the variation in attenuation with current shown in Figure 5.

The equivalent dc circuit is shown in Figure 7, and the equivalent RF circuit in Figure 8, with the diode acting as variable resistors in a normal π network.

The low pass filter was incorporated to provide isolation between the RF circuit and the dc bias current while offering a low resistance path for the variable dc bias current. Isolation could also have been provided through the use of a high resistance bias line. However, this would require a considerably higher bias voltage.

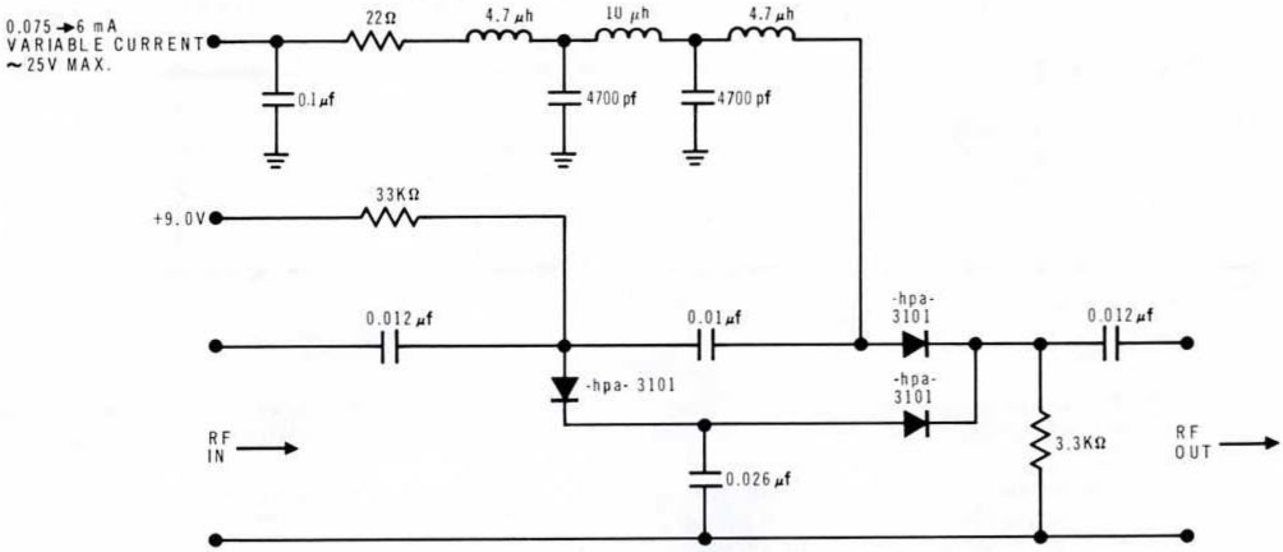


Figure 6

The following curves show the measured results on the final PIN attenuator configuration. Figure 5 is a comparison between the theoretical bias current needed to produce a given attenuation and the actual measured current. The currents shown are those through the two dc branches containing R_1 and R_3. The close correlation between these curves attests to the closeness of the actual diode behavior with the relationship given in equation (1).

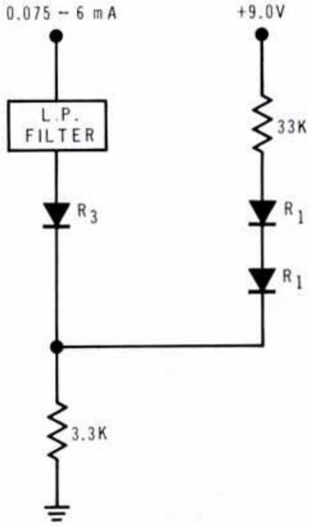


Figure 7

Figure 9 shows attenuation versus frequency for various bias levels and Figure 10 shows the variation of attenuation with bias current. From Figure 9 it may be seen that at the higher attenuation levels (low bias) there is a greater variation in the attenuation level as the full frequency range is covered. Towards the lower frequencies, the rising attenuation with constant bias is due primarily to the increasing reactance of the strip lines blocking capacitors. A portion of this effect can be seen in Figure 11 as increasing VSWR at low frequencies. At high frequencies, the lowering of attenuation (at constant bias) is primarily due to capacitive coupling between input and output. This is due to the diode's parasitic capacitance which turns out to be the limiting factor of high frequency high attenuation operation. In Figure 12 the attenuator's transmission phase shift with frequency is shown. Here again it may be seen that the series transmission mechanism is basically capacitive at the higher attenuation levels.

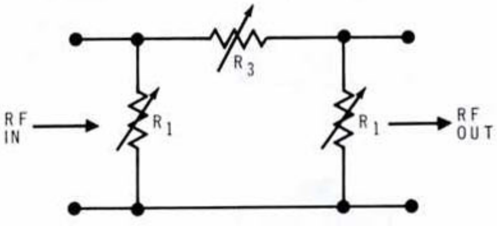
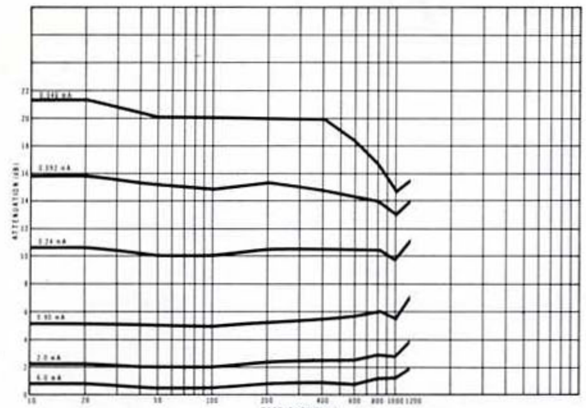


Figure 8

Figures 13a through 13d show the measured output distortion versus the input RF power with bias current as a parameter. At frequencies above 100 MHz, distortion with the power levels shown has dropped considerably and is practically immeasurable. The reason for the output distortion is the non-ideal resistance seen by the RF at lower frequencies. It is in this frequency range (10 to 100 MHz) that the PIN diode's carrier lifetime is not long enough to handle the slower moving RF on its reverse bias variation. If the RF power is high enough, then the stored charge in the intrinsic region will be sufficiently depleted on the negative half cycles to cause partial rectification and hence distortion in the output.

Although a pill package diode was used in the finalized PIN attenuator, there is no reason why this has to be the only choice. The pill was used for convenience in mounting and keeping to an absolute minimum the inductive reactance associated with a packaged diode. An attenuator using glass package diodes such as the HPA 3001 could also be constructed. Small inductive reactances would be inherent in the higher frequencies of operation with a correspondingly larger transmission phase shift and slightly higher VSWR. Any other circuit elements should be ones with the lowest possible parasitic reactances. The package inductance of the HPA 3001 is approximately 3 nhy as compared to the HPA 3101's 0.5 nhy. The electrical performance of these two diodes will otherwise be identical.



Fiaure 9

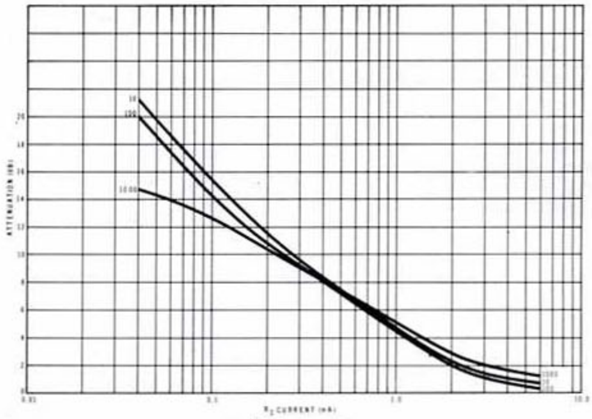


Figure 10

Figure 11

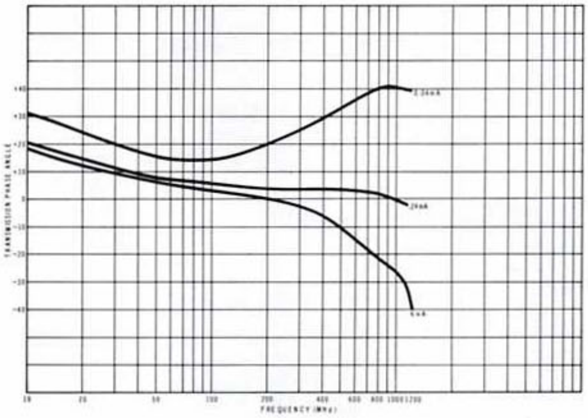


Figure 12

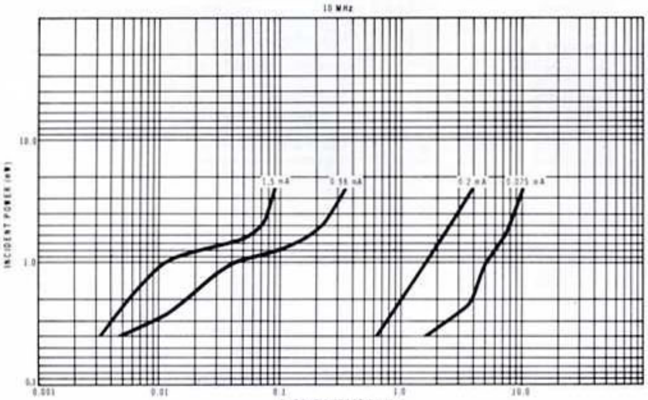


Figure 13a

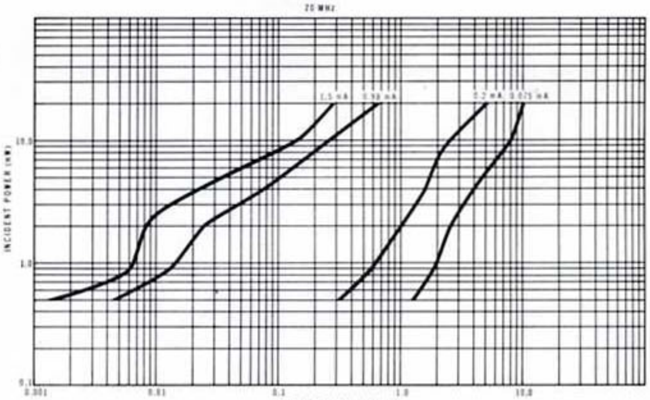


Figure 13b

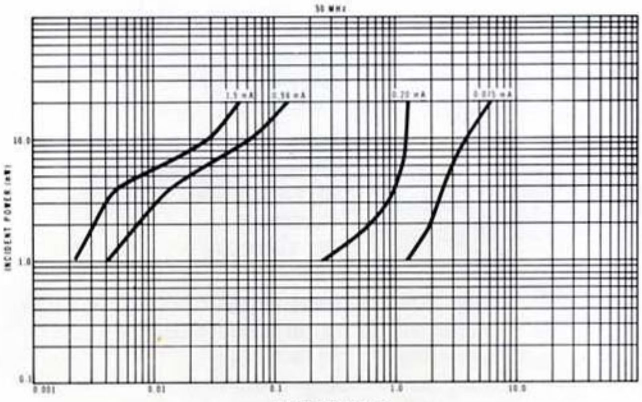


Figure 13c

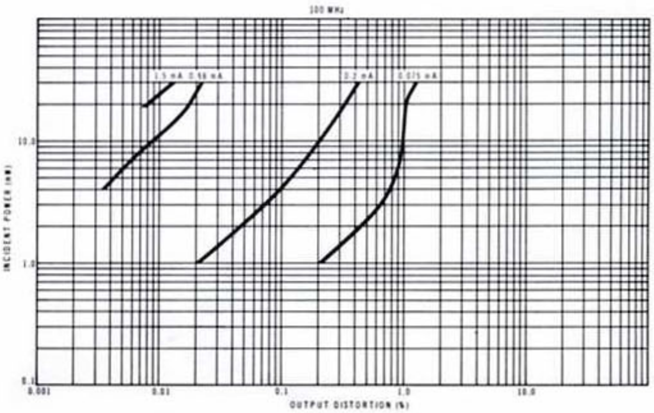


Figure 13d

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