Pulse and Waveform Generation with Step Recovery Diodes
I. Introduction

Since its commercial introduction by HP four years ago, the Step Recovery Diode (SRD) has found many useful applications. One major area of applications is in pulse shaping and waveform generation, which is the subject of this note. The others are in harmonic frequency multiplication and frequency comb generation, both of which are discussed in HP Application Note 920.

In all applications, the SRD is used as a charge controlled switch. For example, when charge is inserted into the diode, by forward bias, the diode appears as a low impedance. When this charge is being removed, the diode continues as a low impedance until all the charge is removed, at which point it rapidly switches from a low impedance to a high impedance. This ability of the SRD to store charge and to change impedance levels very rapidly can be exploited for generating extremely fast rise time pulses and for general waveform shaping.

In pulse applications, the manner in which the diode changes impedance states and the dependence of this characteristic on stored charge is very critical to circuit performance. To assure repeatable performance in pulse applications, the transient characteristics of the SRD must be properly specified and assured by time domain testing.

This note describes in detail what characteristics of the SRD are most critical to pulse applications, how these are controlled and specified, and how the SRD can be used in a variety of pulse shaping and waveform generating circuits.

II. Properties of the Step Recovery Diode

The Step Recovery Diode (SRD) is a two-terminal P-I-N junction, usually silicon, whose static (DC) characteristics are similar to the usual p-n junction diode, but whose dynamic (switching) characteristics are quite different.

The SRD dynamic characteristics are extremely important in switching circuit applications. To be useful, a switching type SRD is precisely controlled during manufacturing and is thoroughly time-domain tested. To be used correctly, a knowledge of these characteristics and how they are specified is a necessary prerequisite.
1. Ideal Dynamic Characteristics

The most distinguishing feature of the SRD is the very abrupt dependence of its junction impedance upon its internal charge storage (Ref. 1). This storage of charge occurs as a result of the non-zero recombination time of minority carriers that have been injected across the junction under forward bias conditions.

The charge stored under forward bias can be obtained from the charge continuity equation

\[ i(t) = \frac{dQ}{dt} + \frac{Q}{\tau} \text{ for } (Q > 0) \]  

(1)

where

- \( i \) = total instantaneous diode current
- \( Q \) = charge stored at junction
- \( \tau \) = minority carrier lifetime of diode

For a constant charging current, the stored charge is:

\[ Q_f = I_f \tau (1 - e^{-I_f/\tau}) \]  

(2)

where

- \( Q_f \) = stored charge from forward current
- \( I_f \) = forward charging current
- \( t_f \) = length of time forward current \( I_f \) is applied

If \( t_f \) is long compared to \( \tau \), then

\[ Q_f = I_f \tau \]  

(2a)

If a constant reverse current is now used to withdraw this stored charge, the time required to do so is:

\[ \frac{t_s}{\tau} = \ln \left( 1 + \frac{I_f}{I_R} \right) \]  

(3)

where

- \( t_s \) = time required to remove the charge stored by \( I_f \)
- \( I_R \) = reverse current

As before, if \( t_f \) is long compared to \( \tau \)

\[ \frac{t_s}{\tau} = \ln \left( 1 + \frac{I_f}{I_R} \right) \]  

(3a)

These relationships are shown graphically in Figure 1.

These simple relationships are fundamental to the understanding of charge flow in an SRD and, although somewhat idealized, are nevertheless very useful in design and analysis of most SRD circuits.

Quite often in many SRD circuits, \( I_f/I_R << 1 \). In these cases, a further simplification of Equation (3) is possible, i.e.,

\[ \frac{t_s}{\tau} \approx \frac{I_f}{I_R} \]  

(3b)

The amount of error incurred by this approximation is shown in Figure 2.

Figure 2. Error for Approximation of \( \frac{t_s}{\tau} = \frac{I_f}{I_R} \)

If a forward biased SRD is suddenly reverse-current biased, it will first appear as a very low impedance (generally less than 1 ohm) until the stored charge is depleted. Then the impedance will suddenly increase to its normal high reverse impedance, thereby stopping the flow of reverse current. This impedance transition generally takes less than a nanosecond. This property of the SRD can be used for generating extremely fast rise time pulses and for sharpening slow rise time pulses. This is illustrated in the circuit of Figure 3.

In this circuit, the battery supplies a constant forward current \( I_f \) which stores charge in the SRD. The pulse generator supplies a positive going voltage step which reverses the diode current, as shown in Figure 3(b).

Due to charge storage during forward conduction, the diode impedance remains low, short circuiting the source for a time designated \( t_s \). This time, called storage time, is measured between the 50% points of the reverse current waveform, or, equivalently, between the 50% points of the output waveforms obtained with and without the diode in the circuit. The storage phase ends when the stored charge is depleted and the diode suddenly becomes an open circuit causing the output of the generator to be applied to the load.
The fall time of diode reverse current, \( t_r \), which also equals the rise time of the voltage on the load, is called the Transition Rise Time. This time is a function of: diode design, circuit constraints, and diode operating conditions.

Figure 3 illustrates one of the most basic circuit roles the diode can take—that of a pulse sharpener. The output rise time \( t_r \) in Figure 2 is clearly faster than the input rise time and is delayed by the time \( t_c \). For a given pulse amplitude and source resistance, \( t_r \) can be adjusted, by varying \( I_p \), to be many times greater than \( t_c \). Therefore, the output rise time of this circuit can be many times smaller than the rise time of the drive waveform. In practice, a 10 ns pulse rise time can be easily sharpened to 300 ps with a one diode circuit, and to 100 or 50 ps with two and three diode circuits. The detailed design of these circuits is given in Section III.

2. Actual Dynamic Characteristics

The output waveform shown in Figure 3(c) is one that would be obtained with an ideal SRD. When a real SRD is used, the presence of diode and package parasitics and the dependence of diode dynamic characteristics on both the circuit and the operating conditions result in a waveform more like that shown in Figure 4(b).

To determine what gives rise to the various parasitic effects evident in this waveform, we must consider the equivalent circuit of a packaged SRD. This is shown in Figure 5.

The first parasitic effect is the voltage drop of the diode under forward bias:

\[ V_F = \phi + I_F R_S \]  \hspace{1cm} (4)

Figure 4. Waveform Across SRD in Test Circuit
(a) Ideal Diode   \hspace{1cm} (b) Practical Diode

Figure 5. SRD Equivalent Circuits
(a) Forward Bias   \hspace{1cm} (b) Reverse Bias

This voltage is typically 0.7 - 0.8 volt. This steady-state voltage will not appear in the output of the circuit in Figure 3 because of capacitive coupling to the load.

The second effect is the voltage spike \( V_L \). This is the result of the rapid change of current through the package inductance and is given as:

\[ V_L, (\text{max}) = L_p \left( \frac{di}{dt} \right)_{\text{max}} \]  \hspace{1cm} (5)

For a typical \( L_p \) of 4 nH and a reverse current of 400 mA occurring in 10 ns

\[ V_L = 4 \, \text{nH} \times \frac{0.4 \, \text{A}}{10 \, \text{ns}} = 0.16 \, \text{volt} \]  \hspace{1cm} (5a)

For faster current fall times, i.e., when sharpening a 1 ns rise time, this voltage will be 1.6 V and may not be negligible. In this case, a diode package with a smaller \( L_p \) should be used. Because of this, diodes with fast transition rise time specifications are generally packaged in low inductance packages. Available packages are shown in Figure 6.
Figure 6. Typical SRD Diode Packages
The special Outline 61 package is a recent innovation by HP. By the use of a three-terminal configuration, shown schematically in Figure 7, the mutual inductance $L_m$, which causes the voltage spike, is greatly reduced—typically to less than 40 pF.

![Figure 7. Three-Terminal Diode Package](image)

The lead inductances $L_a$ remain as before, however these leads can either be geometrically proportioned to form a matched transmission line to the source and load, thereby eliminating any lumped inductive effects, or they can be formed to produce an optimum inductance value for certain applications.

The third parasitic effect is the voltage plateau $V_p$. This is caused by the reverse current component flowing through the dynamic series resistance $R_s$ of the diode during the storage phase, and is given by

$$V_p = (I_f + I_R) R_s$$  \hspace{1cm} (6)

For the circuit conditions used in the previous example, the plateau voltage $V_p$ is:

$$V_p = 410 \text{ mA} \times 0.4 \Omega = 0.16 \text{ volt}$$

and is generally negligible.

The next three effects, those of Ramping, Transition, and Rounding, are due to the dynamics of charge removal. The magnitude of these effects is controlled primarily by the design and material properties of the semiconductor chip, i.e., doping profile, 1-layer width, resistivity, lifetime, and diode geometry, and to some extent by the external circuit and biasing conditions.

Ramping ($R_a$) is almost wholly dependent on the material properties of the chip and only slightly on charge storage. In a typical switching SRD, ramping is usually less than 10%. Because it is slightly dependent on stored charge, it is usually given as a typical $R_a$ vs. $Q$ curve and as a maximum value at a specified charge level.

The transition rise time ($t_r$) is dependent on diode design, circuit constraints, and the level of stored charge. The transition rise time is composed of two components, as follows:

$$t_r = \sqrt{t_r^2 + t_{rc}^2}$$  \hspace{1cm} (7)

where

- $t_r = \text{Intrinsic diode transition time}$
- $t_{rc} = \text{Circuit (RC controlled) rise time}$

The diode intrinsic transition time ($t_{tr}$) is dependent on the level of stored charge and diode design. The circuit controlled rise time ($t_{rc}$) is dependent on the diode reverse biased capacitance and the equivalent circuit resistance in parallel with it. For a 10%–90% specification of rise time

$$t_{rc} = 2.2 \text{ Req } C_{VR}$$  \hspace{1cm} (8)

and for a 20%–80% specification

$$t_{rc} = 1.4 \text{ Req } C_{VR}$$  \hspace{1cm} (9)

where Req is the equivalent resistance consisting of the parallel combination of the source and load resistances.

The total transition rise time is then

$$t_r = \sqrt{t_r^2 + (2.2 \text{ Req } C_{VR})^2} \quad (10\%–90\%)$$

and

$$t_r = \sqrt{t_r^2 + (1.4 \text{ Req } C_{VR})^2} \quad (20\%–80\%)$$

Typical SRD (20%–80%) rise times, as measured in a 50-ohm system (i.e., Req = 25 Ω), are generally between 300 ps and 60 ps, depending on the diode type and the stored charge level. It is usually given as a $t_r$ vs. $Q$ curve and as a maximum value at a specific level of stored charge.

The Rounding ($R_a$) effect is dependent both on the diode design and the level of stored charge. It is generally given as a typical $R_a$ vs. $Q$ curve and as a maximum value at a specified charge level.

The last parasitic effect that can be observed is the overshoot and ringing waveform. This is due to a damped resonance of the diode and package capacitance with the package and stray circuit inductance which is excited by the high frequency components of the rapidly changing diode current. This effect can be minimized by reducing stray circuit reactances, by choosing a diode with a smaller package inductance, and by some special circuit techniques which will be discussed later.

3. Specification and Measurement of SRD Parameters

Unlike rose, all SRD's are not the same, particularly when it comes to their dynamic characteristics. In a poorly designed or used SRD, the effects of Ramping and Rounding can be sufficiently severe to negate its usefulness in fast switching circuits. Because these effects are also dependent on the material properties of the chip, they can vary considerably from diode to diode, due to the variation of the fabrication process from lot to lot, and under some conditions even within the lot. To assure that the important dynamic characteristics are consistently met in each diode, the fabricating process is tightly controlled and each diode is thoroughly time-domain tested for dynamic and some important static characteristics.

Adequate dynamic testing of diodes with transition times on the order of 50 ps requires the use of extremely fast sampling oscilloscopes and extremely sanitary test fixtures which are absolutely free of spurious or parasitic responses. In general, all the normal precautions usually associated with wideband microwave measurements must be exercised. A block diagram of a typical test setup is shown in Figure 8, and an example of a suitable diode test fixture is shown in Figure 9.
The test fixture consists of a 50-ohm "microstrip" transmission line. The test diode is inserted in shunt across the line. This permits the attachment of a 50-ohm pulse generator and a 50-ohm sampling scope across the diode simultaneously. As long as the load and source are matched, the additional lengths of lines result in a delay of the entire waveform without a change in its shape. To assure low reflections on the line, special wideband microstrip transitions are used from the coaxial connectors of the test instruments to the microstrip line. All the other components used in the test setup, such as attenuators, blocking capacitors, and bias networks, must also be broadband matched to the line.

Microstrip is used for the fixture because it provides the lowest inductance connection for any package to a transmission line. It also lends itself well to rapid insertion and withdrawal of the diodes. The ground plane connection of the diode is made via an expandable collet which assures a good, reflection-free, electrical connection and an excellent thermal path. The top of the microstrip line is fitted with a cover of the same material as the line to assure equal wave velocities both above and below the line to prevent dispersion of the wave fronts.

The test circuit used for dynamic testing of the SRD's is essentially the same as shown in Figure 3. The resulting waveforms are shown in Figure 10.

The waveform of Figure 10(a) clearly exhibits the effect of package inductance and the dynamic diode series resistance. The waveforms of Figure 10(b) illustrate the effect of charge storage on the dynamic characteristics of a good switching SRD. The waveform of Figure 10(c) clearly shows the deleterious effects of ramping and rounding in a poor switching SRD.

The specification limits of Ramping \( R_a \), Rounding \( R_r \), and Transition Rise Time \( t_r \) of HP pulse-specified SRD's are based on these waveforms. For clarity, the definition of each of these parameters is shown in Figure 11.

a) Transition Rise Time \( t_r \): This parameter is defined as the time between the 20% and 80% amplitude points of the over-all step amplitude. Because the measurement is made in a test circuit that presents a resistance to the diode, the actual
transition time of the diode, if needed, must be calculated from Equation (11) as:

\[ t_t = \sqrt{t_t^2 - (1.4 \times \text{Req} \times C_\text{VR})^2} \]  

(12)

For the HP test fixture, Req = 25 ohms. The correction is particularly important for diodes with extremely fast transition times or large capacitance values. The corrections are also necessary when comparing measurements made on different test jigs which may present a different resistance to the diode.

The concept of ramping or rounding is an easy one to grasp, but the quantitative measurement of it is very difficult, unless an unambiguous definition is chosen. At HP, the following definitions have been chosen as having the best correlation with subjective judgments of the various waveforms possible, while still being capable of automatic measurement.

b) Ramping: This parameter is stated as a percent of the overall step amplitude. The amplitude of the ramp is defined as the part of the overall step amplitude that lies before the tangent point of the waveform and the “critical” slope line.

c) Rounding: This parameter is also stated as a percent of the overall step amplitude. Its amplitude is defined as the part of the overall step that lies after the second tangent point of the waveform and the “critical” slope line.

The “critical” slope in both of the above definitions is defined to be the slope of a line whose time separation between the 20%–80% points is three times the rise time specification for the particular diode at the specified test conditions.

All HP SRD’s which are intended for use in pulse applications are tested as described above for conformance with the stated specifications. A summary of these specifications for the HP switching SRD’s is shown in Table I.

**Electrical Specifications at \( T_\text{J} = 25 \, ^\circ\text{C} \)**

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<tbody>
<tr>
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<td>( V_\text{BR} )</td>
<td>V</td>
<td>800</td>
<td>1200</td>
<td>1500</td>
<td>1800</td>
<td>1800</td>
<td>2000</td>
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</tr>
<tr>
<td>Series Resistance</td>
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<tr>
<td>Leakage Current</td>
<td>( I_\text{L} )</td>
<td>mA</td>
<td>100</td>
<td>200</td>
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<td>5</td>
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<tr>
<td>Transition Rise Time</td>
<td>( t_\text{R} )</td>
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<td>50</td>
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<td>Rounding</td>
<td>( t_\text{R} )</td>
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<td>Forward Current</td>
<td>( I_\text{F} )</td>
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<td>1000</td>
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<tr>
<td>Reverse Current</td>
<td>( I_\text{R} )</td>
<td>mA</td>
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Note 1: Rounding is not specified for the HP 1002-0802 because of waveform overshoot due to package inductance.

**Table I. Specifications of HP Pulse Specified SRD's**

Since these parameters also depend on the level of stored charge, typical curves of Ramping, Rounding, and Transition Rise Time, as a function of stored charge, are also given as shown in Figure 12.
These curves are used in determining the expected performance of a given diode under circuit conditions that may be far different from the standard test conditions given in Table I. They are also extremely useful in selecting an optimum diode for a particular application. How this selection is made is discussed in detail in Section III.

d) Static Characteristics: In addition to the dynamic characteristics, certain static characteristics of the SRD are also specified to assure repeatability of performance or to provide values for circuit design. The most usual static

Figure 12(a). SRD Dynamic Characteristics
III. Design of SRD Pulse Circuits

1. Pulse Sharpening Circuits

The basic function of a pulse sharpening circuit is to convert a slow rise time or fall time input pulse into a faster rise time or fall time output pulse. A variety of SRD circuits can be configured to perform such a function, depending on the detailed requirements. One of the simplest circuits of this type is the resistive source and load SRD test circuit that was discussed in Section II.

Besides being simple, this circuit also lends itself well to illustrating the fundamental design principles which are used in essentially the same form in more complicated circuits. 

a) Basic Design Procedure: The design usually starts with a knowledge of the input waveform, the desired output waveform, and the source and load resistances. Let us assume the following design specifications:

- **Input Waveform**
  1. Pulse Width: 50 ns (50%—50%)
  2. Rise Time: 10 ns (10%—90%)
  3. Fall Time: 10 ns (10%—90%)
  4. Repetition Rate: 10 KHz
  5. Peak Open Circuit Voltage: 20.5 volts
  6. Peak Loaded Output Voltage (into 50 Ω load): ≈ 10 volts

- **Desired Output Waveform**
  1. Rise Time: < 300 ps (10%—90%)
  2. Load Resistance: 50 Ω
  3. Peak Load Voltage: 10 volts

Based on the analysis in Section II, we assume that a simple SRD sharpener circuit, as shown in Figure 13, will suffice and that the expected waveforms in this circuit will be as shown in Figure 13(b), (c), and (d).

First, the proper diode must be chosen. Since clipping of the output amplitude is not desired, the breakdown voltage of the diode must be:

\[ V_{BB} > E_{max, p} = 10 \text{ volts} \]

This value is well within the limits of any of the available diodes shown in Table I.

Because the transition time of the diode is dependent on stored charge, we next determine the minimum stored charge that is required. The storage time \( t_s \) should be equal to or slightly greater than 1/2 the input rise time. We take

\[ t_s = \frac{1}{2} t_r \]

If \( t_s \) is < 1/2 \( t_r \), then the diode will transition prior to completion of the rise time. Only a portion of the rise time will be sharpened. If it is much greater than 1/2 \( t_r \), there will be a greater delay (which may not be desirable) and the output rise time will be slower since the transition time of the diode increases with stored charge.

Figure 12(b). SRD Capacitance vs. Bias

characteristics and the methods of measurement, at 25°C, are summarized below.

- **V_{BB}** (reverse breakdown voltage) — This is measured under a fixed applied reverse current, usually 10 μA. \( V_{BB} \) has importance in two ways. First, it must be greater than the peak applied voltage to avoid unwanted amplitude limiting. Second, this voltage is related to internal geometry, and hence to transition time of the diode.

- **C_{VR}** (reverse bias capacitance) — This is the total capacitance of the diode and includes both the package capacitance \( C_p \) and the junction capacitance \( C_j \). The measurement is made at 1 MHz under small signal conditions and with the diode reverse biased, usually at —10 volts. The capacitance of an SRD is quite constant for reverse bias greater than 1/10 of \( V_{BB} \). The choice of a standard of —10 volts is therefore suitable for most SRD's.

- **R_s** (series resistance) — This is the effective ac (slope) resistance of the diode when it is biased well into forward conduction. The measurement is made by applying a small 1 kHz signal from a constant current source and measuring the resulting ac voltage drop across the biased diode.

- **I_L** (leakage current) — This is the diode leakage current when reverse biased about 75% of \( V_{BB} \). It is a measure of the quality of the reverse avalanche characteristics.

- **I_{Qo}** (forward current at stored charge) — This is a measure of the forward current required to produce a specific level of stored charge. Under steady state conditions, the stored charge \( Q_s = I_T \tau \) where \( \tau \) is the minority carrier lifetime. However, \( \tau \) is generally not a constant, but depends on the level of stored charge. Since in normal design and diode operation, it is the level of stored charge that is of interest, consequently it is more useful and convenient to specify the current as a function of stored charge than it is to specify \( \tau \). Typical curves of \( I_{Qo} \) vs. \( Q \) are shown in Figure 12(a).
The stored charge that is removed by the reverse current is the area under this curve. For this case:

\[ Q_S = \frac{t_r I_R}{2} = \frac{10 \, \text{ns} \times 400}{2} = 2000 \, \text{pC} \]

Any SRD which is to sharpen the given waveform must store at least 2000 pC.

From the design specifications, we know that the rise time must be < 300 ps. The diode transition time is related to the circuit rise time by Equation 10.

\[ t_r = \sqrt{t_u^2 + (2.2 \, \text{Req} \, C_{VR})^2} \]

It should be noted that \( t_r \) cannot be minimized by choosing a diode with a small \( C_{VR} \) since such a diode will generally have a higher \( t_r \) at the same charge level. Generally minimum \( t_r \) occurs when \( t_r = 2.2 \, \text{Req} \, C_{VR} \). Assuming that the circuit blocking capacitors \( C \) are large, then the equivalent resistance \( \text{Req} \) shunting the diode capacitance \( C_{VR} \) during transition is:

\[ \text{Req} = \frac{R_L \times R_g}{R_L + R_g} = \frac{50 \times 50}{100} = 25 \, \text{ohms} \]

Since this resistance is the same value as is used in testing the diode, then the required diode can be simply selected from the \( t_r \) vs. \( Q \) curves of Figure 12 or the \( t_r \) specifications given in Table I.

If the equivalent resistance for this circuit were not 25 ohms, then the required diode rise time as specified in Figure 12, at 2000 pC must be:

\[ t_r^2 \leq t_u^2 + (2.2 \, C_{VR})^2 (625 - \text{Req}^2) \]

where:

- \( t_r \) = required circuit rise time
- \( t_u \) = diode rise time (as stated in the specifications)
- \( \text{Req} \) = equivalent resistance of the circuit

If \( t_r^2 \) comes out negative, a lower capacitance diode must be chosen.

From the curves of \( t_r \) vs. \( Q \), we see that either the HP 5082-0202 or the 5082-0200 is suitable, since both are specified to operate at the required charge storage level and the specified maximum \( t_r \) is less than 300 ps.

Since the circuit rise time was specified at the 10%–90% points, the next criteria would be Ramping and Rounding. From the curves of Figure 12, we see that only the 0220 diode satisfies both requirements with a ramping of 10% and negligible rounding.

Having selected the diode, we now have to determine the forward bias current, the required input pulse amplitude, and the effect of the series resistance and package inductance on the output pulse shape.

The forward current is obtained from the curve of Figure 12(a) \( I_{QV} \) vs. \( Q \) and is \( = 10 \, mA \) for a stored charge of 2000 pC. This corresponds to an effective minority carrier lifetime of

\[ \tau = \frac{Q}{I_f} = \frac{2000 \, \text{pC}}{10 \, mA} = 200 \, \text{ns} \]

This is substantially greater than the required storage time.
of 10 ns, therefore we can expect a negligible loss of charge from internal recombination.

The required input current step amplitude is:

\[ I_{sa} = I_i + I_n = 410 \text{ mA} \]

The required generator open circuit voltage is:

\[ E_{(dec)} = I_{sa} \times R_s = (410 \text{ mA}) \times (50 \Omega) = 20.5 \text{ volts} \]

The inductive spike at the start of the output pulse is due to the package inductance. For the 0202 diode, the package inductance is \( \approx 4 \text{ nH} \). Assuming the source has a linear rise time between the 10%—90% points, then:

\[ V_L = L_p \frac{di}{dt} = 4 \text{ nH} \times \frac{330 \text{ mA}}{10 \text{ ns}} = 0.132 \text{ volt} \]

The plateau voltage \( V_p \) following the inductive spike is due to the series resistance \( R_s \) of the diode. For the 0202, \( R_s \) is 0.4 ohm, therefore:

\[ V_p = I_n R_s = 410 \text{ mA} \times 0.4 \text{ ohm} = 160 \text{ mV} \]

Since the diode package inductance is 4 nH, it is worth while checking if the leading edge will exhibit an overshoot and ringing. The peak overshoot voltage can be estimated as shown in Section III (5a). For the 0202 diode, \( L_p = 4 \text{ nH}, C_{VR} = 4 \text{ pF} \), therefore the damping factor is:

\[ \zeta = \frac{Z_0}{4} \sqrt{\frac{C_j}{L_p}} = \frac{50}{4} \sqrt{\frac{4 \times 10^{-10}}{4 \times 10^{-9}}} = 0.4 \]

From Figure 53, the peak overshoot will be \(< 20\%\), or \(< 2\text{ volts}\).

To complete the design, we must finally investigate the stability of the leading edge (pulse jitter) and the repetition rate limit of the circuit.

Pulse jitter will occur if \( t_n \) is not constant. Since

\[ t_s = \tau I_i / I_n = \tau \frac{I_n R_s}{E_g} \]

jitter can occur due to variation in \( \tau \), and amplitude changes in both the bias supply and the input pulse. For short term variations, \( \tau \) can be considered constant. Any ripple or noise in the bias supply and the input pulse will produce a proportional change in \( I_i \). For a 1% peak-peak amplitude change in either, the leading edge jitter will be \((0.01)(5 \text{ ns}) = 50 \text{ ps}\).

Maximum repetition rate will be limited due to the time required to build up the stored charge in the diode after each pulse. The charge buildup in the diode is given by:

\[ Q_r = I_r \tau (1 - e^{-t/F}) \]

For a 5% variation in \( Q_r \) and a nominal lifetime of 200 ns, the minimum charging time will be:

\[ t_r = \tau n(1/0.05) = 200 \times 3 = 600 \text{ ns} \]

With a 50 ns pulse, the maximum repetition rate will be 1.54 MHz.

The coupling capacitors “C” used in the circuit will generally impose a more severe limit on the maximum repetition rate.

This calculation is straightforward and will not be covered here in detail. Qualitatively, there will be some sag in the output pulse, and some charge buildup on the capacitors. This charge will help “spike” the diode forward current at the trailing edge of the input pulse, adding some extra charge; however it will take some time to reach its equilibrium value, around \((5)(R_s)(C)\).

This essentially completes the design and analysis of a simple pulse sharpening circuit. Additional circuits that eliminate some of the problems encountered above, or which perform more complicated pulse sharpening functions, are discussed below.

b) Direct Coupled Pulse Sharpener: The circuit shown in Figure 15 eliminates the capacitor recovery problems encountered in the circuit of Figure 13, by not having any.

![Figure 15 Direct Coupled Pulse Sharpener](image)

The penalty paid, however, is the need of a larger bias current and slightly worse temperature stability. The required bias current is

\[ I_{b'} = I_i + \frac{\phi}{25} = 10 \text{ mA} + 28 \text{ mA} = 38 \text{ mA} \]

The temperature coefficient of \( t_s \) is already positive since \( \tau \) increases with temperature at \( = 1/2\% /{^\circ}C \). The diode forward voltage \( \phi \) decreases with temperature. This results in an increase in \( I_i \) and an addition to the positive temperature coefficient of \( t_s \), which may be objectionable.

c) Diode Coupled Pulse Sharpener: Another modification to the circuit of Figure 13 is the replacement of capacitors with silicon switching diodes, as shown in Figure 16.

![Figure 16 Diode Coupled Pulse Sharpener](image)

Here \( CR_1 \) is a fast recovery diode (FRD) which prevents loss of a significant part of the bias current \( I_i \) into the source,
due to its forward $V-I$ characteristic, but allows the much higher signal pulse to pass almost unattenuated. $CR_3$ is back-biased by the forward voltage of $CR_2$, and becomes forward-biased by the pulse, allowing it to get through.

Use of silicon diodes in this way is possible in many of the circuits described in this note, and allows deletion of capacitors, which take up space, add inductance, and limit maximum repetition rate.

A useful diode in this application is the HP 5082-1002 (800 mA at 1.4 V forward, 3 pF capacitance) or the HP 5082-1001 (500 mA at 1.4 V forward, 1.5 pF capacitance). These are fast silicon P-N junction switching diodes. If faster recovery times are required for extreme applications, a hot carrier diode (HCD) such as the HP 5082-2520 can be used; however, due to the lower forward drop of a HCD ($= 0.4 V$), two in series will be needed for $CR_1$.

d) Inductive-Drive Pulse Sharpener: The presence of circuit and diode parasitic reactances in the circuit of Figure 13 will generally result in some overshoot and ringing on the leading edge of the output pulse, as was shown in Figure 4.

The exact shape of the overshoot waveform depends in a complicated way on the values of the parasitic elements and their distribution which take the general form shown in Figure 17.

![Figure 17. Typical Distribution of Parasitic Elements](image)

If the source is not truly resistive, but is a combination of $R$, $L$, and $C$, as is often the case, a small circuit modification can help greatly. This involves replacing the generator impedance by a pure inductance, as in Figure 18.

![Figure 18. Inductive Drive Pulse Sharpener Circuit](image)

**Figure 19. Inductive Drive Pulse Sharpener Waveforms**

Neglecting saturation voltage drop in the transistor and forward drop in the fast recovery diode (FRD), operation is as follows:

The transistor is driven into saturation by a drive transformer. When driven by a constant base current, a transistor is capable of sustaining a collector current linearly increasing with time. (See Figure 20 for a quick summary of transistor pulsed current behavior.)

If $\frac{di}{dt} = E_{sd}/L$ is less than the current-time slope the transistor can sustain, the transistor will quickly saturate, and the current will be determined by

$$i_t = \frac{1}{L} \int E_{sd} dt,$$

as shown.

When $i_t = E_{sd}/R_L$, the SRD should snap, and the current $i_t$ switches from the SRD to $R_L$ with a completely flat top. If the SRD snaps late, $i_t > E_{sd}/R_L$, causing an output overshoot as shown dotted in Figure 19. The time at which it snaps is controlled by $I_p$, which sets the stored charge, so this must be properly adjusted to eliminate any L-R transient if a flat top is desired on the output step. This circuit works well mainly because a saturated transistor is inductive, therefore, an additional inductor of several hundred nanohenries is easily added and the combination acts like a "good" inductor.

Aside from the difficulty of constructing a purely resistive source, there is a basic 2:1 charge level advantage of the inductive drive circuit over the equal-resistance resistive circuit. For example, for a 10-volt output, the peak reverse
current for the inductive drive is 200 mA as compared to 400 mA for the resistive drive.

Assuming equivalent current rise time drive amplifiers (so storage times are equal), the diode stored charge is half for the inductive circuit. The resistive and inductive feedthrough is also half due to lower diode currents.

e) Multiple Stage Pulse Sharpeners: It is possible that a single optimized shunt SRD step sharpener stage will not produce a fast enough rise time output for the given input pulse rise time. The basic cause for a dependence of output rise time on input rise time is the slope of the $t_r$ vs. $Q$ curves. As indicated previously, other things being held equal, an increase in input rise time requires a greater storage time ($t_s$) and a greater stored charge ($Q$), causing an increase in output rise time. If this is excessive, multiple stage sharpening can be used. In a properly designed multiple stage sharpener, the fast reverse current fall in one diode is transferred into a reverse current rise of the next diode, resulting in a much lower stored charge, hence a lower optimized $t_s$ in the next diode. With two stages, a 10 ns rise time, 0.4 ampere pulse can be sharpened to less than 100 ps rise time. With three stages, less than 50 ps is possible.

The design of multiple stage sharpeners is done stage by stage, starting at the output end, and using the procedure outlined previously. In addition, some consideration must be given to interstage coupling.

Since $CR_1$ is a high capacitance large-area device, it cannot be directly shunted across $CR_2$, a low capacitance device, without slowing the transition of $CR_2$ excessively.

Some coupling methods that have been found useful are shown in Figure 22.

2. Pulse Shaping Circuits

The basic function of an SRD pulse shaping circuit is to sharpen both the rise and fall time of an input pulse. There exists a large number of such circuits consisting of series diodes, shunt diodes, and their combinations. Two of the most important circuits of this class are described below. Since the methods of analysis for these circuits are similar for the basic pulse sharpener circuits covered previously, only their unusual design features will be discussed.
a) Shunt-Series Pulse Shaper: The basic circuit and its waveforms are shown in Figure 23. In this circuit, \( CR_1 \) acts as a simple shunt sharpener. Initially, \( CR_2 \) as biased by \( I_{f_2} \), remains a short circuit, and the fast rise of \( CR_2 \) becomes the leading edge of the output pulse. During the duration of the output pulse, \( CR_2 \) is supplying load current as a reverse current, depleting its stored charge. When \( CR_2 \) is depleted of charge and open circuits, the load becomes disconnected from the source and a fast fall time of load current occurs. \( I_{f_1} \), essentially controls output pulse delay, and \( I_{f_2} \) controls output pulse width, with the restriction that the input pulse width must be greater than the output width plus the delay. Example:

\[ E_{adj, m} = 20 \text{ volts open circuit, } 10 \text{ volts into } R_L \]

Input pulse width > 20 ns

\[ R_s = R_4 = 50 \Omega \]

\[ CR_1, CR_2 = \text{HP 5082-0202 SRD's} \]

Input \( t_r = t_f = 10 \text{ ns} \)

Output pulse width = 10 ns

Find: \( I_{f_1}, I_{f_2} \) and output rise and fall time.

\[
10 \text{ ns} = \ln \left( 1 + \frac{I_{f_2}}{200 \text{ mA}} \right)
\]

Solving,

\[ I_{f_2} = 200 \text{ mA} \left[-1 + e^{10/200}\right] = 10.3 \text{ mA} \]

(This assumes that \( \tau = 200 \text{ ns} \) = constant, for convenience.)

Since \( Q_x = (200 \text{ mA}) \times (10 \text{ ns}) = 2000 \mu \text{C} \), then \( t_f = 180 \text{ ps} \).

In calculating the R-C component of pulse fall time, note that the impedance facing \( CR_2 \) is 100 ohms, not the 25 ohms facing \( CR_1 \). So

\[
R-C \text{ fall time} = (2.2)(100)(4 \mu \text{F}) = 880 \text{ ps}
\]

\[
t_f \text{ total} = \sqrt{(880)^2 + (180)^2} = 910 \text{ ps}
\]

This is rather slow, and could be improved by choosing a lower capacitance diode for \( CR_2 \), such as the HP 5082-0200, if desired.

b) Shunt-Shunt Pulse Shaper:

In Figure 24, \( CR_1 \) acts as a conventional shunt sharpener. \( CR_2 \) is back-biased in the absence of an input pulse. When the input pulse is present, it is first shorted out by \( CR_1 \), then sharpened by the transition of \( CR_1 \) forming the leading edge of the output pulse. The operation of \( CR_2 \) depends on the output voltage being large enough to exceed \( E_c \), thus passing forward current through \( CR_2 \) during the output pulse, storing charge in \( CR_2 \) while \( CR_2 \) acts as an output clipping diode. When the input voltage \( E_o \) goes to zero, the output will continue, due to reverse current through \( CR_2 \) supplied by battery \( E_c \). The length of time it continues is the storage time of \( CR_2 \) which is determined by forward current, reverse current, and lifetime of \( CR_2 \) according to Equation 3. This circuit has advantages over that of Figure 23 when the pulse width becomes very wide or when irregularities in the flat top of the pulse must be flattened out. It has disadvantages in that a possible undamped resonant loop exists around \( CR_1, CR_2 \), and the dc source. The loop inductance will form a ringing transient with the capacitance of the back-biased diode following any fast transition, which will be evident unless the loop inductance is reduced below 1 nH. One useful technique for achieving a low value of inductance involves using low-inductance ceramic-packaged...
diodes and metallized ceramic capacitor wafers as illustrated in Figure 25. To achieve this configuration, at least one post of the standard ceramic package (Outline 31) must be machined off.

Figure 25. Low Inductance Technique for Circuit of Figure 24

3. Waveform Generating Circuits

In addition to the basic pulse sharpening and shaping circuits, a variety of other useful and extremely fast waveform generating circuits are possible using SRD’s. The following are examples of a few important ones:

a) Basic Charge-Trading Pair Circuit: A very basic and useful waveform shaping circuit is the charge-trading pair circuit shown in Figure 26.

Figure 26. Basic Charge-Trading Pair Circuit

If \( CR_1 \) and \( CR_2 \) are SRD’s of identical lifetime, and if \( i_0 \) remains positive for a long time, the charge in \( CR_1 \) would be \( \tau I_x \), and the charge in \( CR_2 \) would be zero. If \( i_0 \) were negative for a long time, \( CR_2 \) would have a charge \( \tau I_x \), and \( CR_1 \) would have zero charge. If \( e_0 \) were zero, \( CR_1 \) and \( CR_2 \) would share \( I_x \) and each would have a stored charge of \( \tau I_x/2 \). In every case, for any steady value of \( i_0 \), the total stored charge in \( CR_1 \) and \( CR_2 \) together must remain at \( \tau I_x \). If \( i_0 \) is time-varying, for example a sinewave, the total stored charge \( (Q_1 + Q_2) \) remains at \( \tau I_x \), and merely flows from \( CR_1 \) to \( CR_2 \) and back with each cycle of operation. When the area under each half-cycle of the source current waveform exceeds \( \tau I_x \), the charge will be completely transferred every cycle, even if the input period is much smaller than \( \tau \). This results in the waveforms shown in Figure 27.

Figure 27. Waveforms for Circuit of Figure 26

b) Bi-Directional Impulse Generator: The bi-directional impulse generator circuit will convert a sinusoidal high frequency signal into a train of positive and negative impulses with very fast rise times and precisely controlled 180° spacing. This circuit can be used as a set and reset clock in high speed logic. Because the circuit operates from a sinusoidal input, the required fast rise time clock waveform can be generated where it is required in the system, thereby avoiding waveform degradation and interference problems that would normally arise in distributing a high speed clock around a system.

Figure 28. Bi-directional Impulse Generator
\( i_a = (i_t - i_s) \) is a forward current for \( CR_1 \) and a reverse current for \( CR_2 \). All the charge that was in \( CR_2 \) at \( t = 0 \) is being transferred by \( i_s \) from \( CR_2 \) into \( CR_1 \). At \( t = t_s \), the charge in \( CR_2 \) reaches zero and \( CR_2 \) suddenly becomes a 5 pF capacitor instead of a short circuit. By this time \( i_s \) has decayed practically to zero from the last cycle of operation, so \( i_s = i_{t_0} \).

All the stored charge in the second stage is in \( CR_4 \), so \( v_s \) can’t go positive. The input voltage \( e \) can be considered to be zero during the time interval \( t_1 - t_2 \), since the transient amplitude of \( v_1 \) is large compared to the input at this instant.

The equivalent circuit shunting \( CR_2 \) at this time is shown in Figure 30.

![Figure 30. Equivalent Circuit of First Stage](image)

The transient waveform that occurs due to \( CR_2 \) opening takes \( i_t \) to zero with a half cycle (\( \pi/2 \) to \( 3\pi/2 \)) sinewave shape, and transfers \( i_s (t_s) \) to \( L_2 \) at \( t_2 \) so that \( i_s (t_2) = i_t (t_s) \). Meanwhile, \( v_1 \) goes from zero to

\[ i_t (t_s) \frac{\sqrt{L'}}{C} \]

and back to zero in a half cycle (zero to \( \pi \)) sinewave pulse, where

\[ L' = \frac{L_1 L_2}{L_1 + L_2} \]

Since \( i_t = 0 \), therefore \( i_s (t_2) = i_s (t_2) \) and is negative. This turns on \( CR_2 \) (zero stored charge) and passes reverse current through \( CR_1 \) (full stored charge) so \( v_1 \) remains zero for a while.

The equivalent circuit, as seen by the second stage, is shown in Figure 31.

![Figure 31. Equivalent Circuit of Second Stage](image)

Since \( CR_4 \) has full stored charge at \( t = t_2 \), this polarity of \( i_s \) causes no change in \( v_2 \) for a while. At time \( t_2 \), when \( CR_4 \)
runs out of stored charge, a transient at \( v_2 \) occurs. Since

\[
R_k < \frac{1}{2} \sqrt{\frac{L}{C_{R}}},
\]

this transient is overdamped and \( v_2 \) has the fast rise and exponential drop shown in the last waveform.

Since \( t_2 \) is a component of \( t_3 \), the exponential drop in \( i_2 \) affects \( t_3 \). This effect on \( t_3 \) was considered earlier in the analysis of the first stage.

The description above covers the positive half-cycles of operation. The negative half-cycles are identical, but with all the signs of voltages and currents reversed, and the roles of the upper and lower diodes reversed.

From the waveforms shown, it is seen that the width of the voltage pulse \( v_1 \), and hence the rise time of the current \( i_2 \), is considerably quicker than the slow sinewave buildup time of \( i_1 \) in \( L_1 \), due to the action of \( CR_1 \) and \( CR_2 \). The pulse width of \( v_1 \) and the current rise time is one-half period of the resonant frequency of \( C_1 \) and \( L' \). Since \( C_1 \) is rather large (as it must be in a diode designed for large storage), this time cannot be made arbitrarily small. The second stage diode reverse current waveform has the same speed as the rise time of \( i_2 \), which allows \( CR_3 \) and \( CR_4 \) to operate at a much lower stored charge level. \( CR_3 \) and \( CR_4 \) can then be fast diodes of low capacitance, giving a very small output rise time. In this example, the output circuit has been purposely overdamped. This eliminates energy carryover from one output cycle to the next, thereby simplifying the description considerably. This is not, however, a necessary condition for operation.

The above analysis assumes equal lifetimes for the two diodes in each stage. It can be shown that this is not an essential condition for proper circuit operation.

This circuit is capable of operating over a broad frequency range in a swept mode, if the following requirements are met. First, the short circuit current of the driving source (with \( CR_1 \) and \( CR_2 \) shorted) must be constant vs. frequency. Second, the first-stage recombination current \( I_r \) must be modulated proportional to the period of the waveform, since the stored charge required is proportional to area under the current curve for switching at the peak of the waveforms at all frequencies. The second stage current \( I_p \) is determined by the pulse width \( v_1 \), which is constant, and its height, which should be constant, so \( I_p \) need not be modulated.

**Effect of Parasitic Elements**

In the above discussion, it was implicitly assumed that all four diodes were "ideal." They have zero series resistance and zero internal transition time. The zero series resistance assumption permits the voltage \( v_1 \) to be zero between pulses. If some resistance (\( R \)) is present in \( CR_1 \) and \( CR_2 \), a voltage \( R_{i_2} \) is superposed on voltage \( v_1 \). This voltage is of such a polarity that it starts transferring charge prematurely in the second stage; that is, this "feedthrough" voltage is in the same polarity that the next spike in \( v_1 \) will be. This affects the current waveform of \( i_4 \) in the last stage diodes, as shown in Figure 32.

Although the current plateau caused by the "feedthrough" is small in amplitude, it exists over a relatively long period of time, and its time integral (charge) can be significant. This represents additional charge that must be stored in the final stage diodes to give a transition at the right time, and can easily double the actual charge required over the design value which may be calculated assuming no final stage current until the first stage switches. The additional charge causes slow switching of the final stage by pushing the operating point further to the right on the \( t_1 \) vs. \( Q \) curve.

A very simple and effective method exists for eliminating this problem, at least for the case where only one polarity of output step is needed. The solution is to dc bias the last stage such that the uncharged diode is back biased during the storage time of the first stage.

This bias can be put in location A, B, or C as shown in Figure 33.

**Figure 32. Current Waveform in Last Stage Diodes**

Consider the case where it is at B only. Voltage waveform \( v_1 \) will be offset (\( \pm \)) by \( E_1 \) volts, as shown in Figure 34. During the time between \( t_3 - t_4 \), while \( v_1 \) is sagging in a negative direction, it is biased positively by \( E_1 \), so that the resultant never goes (\( - \)) negative before the first stage switches. This results in \( CR_1 \) being back biased slightly, and no current \( i_4 \) flows until the first stage switches, at \( t_3 \). On the positive half-cycle however, \( v_1 \) goes positive as soon as \( CR_1 \) conducts, clearing the charge out of \( CR_4 \) (second stage) before \( CR_2 \) in the first stage switches off. This causes a much smaller amplitude switching from \( CR_1 \) in the positive direction than from \( CR_3 \) in the negative direction.
The results are similar if the bias is introduced at point A or point C. The bias must be bigger than the peak \(iR\) drop in \(CR_1\) and \(CR_2\), so as to keep \(CR_1\) cut off until \(CR_1\) switches. There is a disadvantage to using an excessive bias, however. During the storage time of \(CR_3\) (see Figure 34), while the voltage drop across the first stage is practically zero (between \(t_2\) and \(t_3\)), all the energy for the output pulse is stored in \(L_2\). This energy is being dissipated in the bias battery, because the bias is essentially right across the inductor during this time, and the inductor’s current is dropping at a rate

\[
\frac{di}{dt} = \frac{E_1}{L_2}
\]

This causes little trouble if the storage time of the last stage is short, as it should be. But if the input drive amplitude to this whole circuit drops, the peak amplitude of \(i_s\) will drop. \(I_n\) is constant, and therefore the stored charge in the last stage is constant. With a drop in drive current amplitude, but a fixed stored charge, the storage delay of the last stage increases, giving the inductor more time to dissipate its energy in the bias supply. This results in an output amplitude loss considerably greater than the amount of drive reduction. This can be minimized by using only as much bias as necessary. A good test for proper bias is to check the value of \(I_n\) necessary to give proper operation. If an increase in \(E_1\) considerably reduces \(I_n\) required, then \(E_1\) wasn’t enough, and charge was being wasted. Another test involves observing the output waveform on an oscilloscope and gradually increasing \(I_n\) from zero. With \(I_n = 0\), the spikes of \(v_1\) will be present at the output. As \(I_n\) is increased, the leading edge of these spikes should immediately start becoming faster, until at optimum \(I_n\) the whole leading edge will be fast. If considerable \(I_n\) is necessary to delay the second stage switching to the point where it occurs after the first stage, \(E_1\) is not enough, and significant last stage charge is being wasted.

**Condensed Preliminary Design Procedure**

The specifications for the circuit should include:
- Desired Peak Current: \(i_{up}\)
- Desired Peak Voltage: \(V_{up}\)
- Desired Load Impedance: \(R_L\)
- Desired Output Rise Time: \(t_r\)
- Desired Pulse Shape and Damping Factor

Characteristics of available current waveform from driving source.

The design starts with the output stage and the selection of the output diode. The equivalent circuit, as seen by the output diode, is shown in Figure 35.

![Output State Equivalent Circuit](image)

**Figure 35. Output State Equivalent Circuit**

Only the overdamped case will be considered. The capacitance of the output diode should be approximately

\[
\frac{t_r}{4.4R_L} < C < \frac{t_r}{3.1R_L}
\]

This balances the two components of \(t_r\) about equally between the diode transition time and the \(R_tC\)-limited rise time. The diode transition time should be between

\[
\frac{t_r}{2} = \frac{t_r}{1.4}
\]

The diode breakdown voltage should be slightly greater than \(V_{up}\). A diode with very large \(V_{hit}\) will generally be slower in transition. Other parameters of the diode, such as \(R_D\), \(\tau\), and \(L_D\), will generally be commensurate with the specified transition rise time, and should only be specified if absolutely necessary. If a diode with the required transition time is not available, a slower diode can be used and the \(R_tC\)-limited rise time can be decreased by a factor of about 1.5 by the addition of the proper amount of stray inductance between the diode and the load. This can be determined by experiment.

Next, \(L_2\) can be chosen to give the desired damping factor in the \(L-C-R_T\) circuit and the output waveform from:

\[
\zeta = \frac{R_T}{4} \sqrt{\frac{C}{L_2}}
\]
The available drive current waveform must be evaluated as to the charge required to achieve diode switching at the desired point on the waveform. If this is not above the maximum charge at which the output stage can still give the desired output rise time (see $I_c$ vs. $Q$ curves of Figure 12), one stage will suffice. Otherwise, a first stage using larger area devices must be used. The first stage diode capacitance must be small enough so that the current rise time

$$I_r = \pi \sqrt{\frac{L_2 C}{2}}$$

is fast enough to insure low charge storage operation of the last stage.

The inductors need not be made equal, but a current loss will occur in the first stage if $L_2 > L_1$, and a gain will occur if $L_1 > L_2$. The drive source must develop the required current waveform in the first inductor, as well as supply a dc path across its own terminals.

DC bias currents can be estimated from the design charge storage level using curves of Figure 12. Since a 3:1 range of lifetime variation will occur in production, these supplies must be adjustable over a wide range.

This procedure will result in a rough design that will get the circuit operating. Refinements are probably best made on the basis of measurements on this trial circuit.

c) Square Wave Generator: Another shunt SRD circuit using an inductive drive and two SRD's in shunt with the output load, is shown in Figure 36.

This circuit converts a sinusoidal input into a square wave output with very fast rise times, as shown in Figure 37. The duty factor of the output can be readily adjusted by varying the bias. The conversion efficiency is on the order of 90% – 50%, depending on the input frequency and rise time required. The circuit is capable of operating at frequencies from 10 to over 500 MHz. This circuit is highly suitable as a high frequency timing clock in logic circuits, as a driver for high speed sampling gates, or as a high speed square wave test generator.

Proper operation of this circuit will occur if:

$$E_1 \gg V_1, V_2$$

$$\frac{E_1}{\omega L_1} > \frac{2}{(V_1 \text{ or } V_2)} \left( \frac{R_2}{R_L} \right)$$

and

$$\frac{2\pi}{\omega} \ll \tau$$

The capacitors $C_1$, $C_2$, and $C_3$ are very large bypass capacitors for applied dc voltages $V_1$, $V_2$, and $V_3$. $CR_1$ and $CR_2$ are SRD's of long lifetime compared to the period of the sinusoidal excitation. $L_1$ is a large inductor whose impedance is many times $R_2$ at the operating frequency. $L_2$ is a very large inductor and is used to introduce the bias voltage $V_2$ on the junction $A$. $V_1 > V_2 > V_3$ always remains true. $R_2$ determines the output impedance of this circuit and would typically be in the range of 50–100 $\Omega$.

To simplify the analysis of the circuit, $CR_1$ and $CR_2$ are assumed to have zero voltage drop during forward conduction and charge storage. They are also assumed to have infinite lifetime, so that all the charge stored by forward current must be displaced by reverse current before a diode switches “open” in each cycle. If $X_{1A}$ and $E_1$ are both very large, the current $i_t$ flowing into point $A$ is close to sinusoidal. Assume the output is open-circuited. Obviously, the large instantaneous current $i_1$ must flow either through $CR_1$ or $CR_2$ at every instant. Therefore, the instantaneous voltage at $A$ must be either $V_1$ or $V_2$ at all times. The average voltage at $A$ must however be $V_3$ due to $L_2$. The only possible waveform that satisfies these requirements is a pulse waveform at $A$ which switches between $V_1$ and $V_2$, and whose duty factor is such that its average value is at a voltage $V_3$.

The waveforms can be easily drawn for the case where $V_1 = -V_2$, $V_3 = 0$. This requires a square wave of positive peak + $V_1$, negative peak –$V_1$, and zero dc component. The only question remaining is the phasing of the output square wave compared to the input current $i_t$. This is fixed by the fact that neither diode can pass any dc current due to total recovery of stored charge, and the known fact that they must switch every cycle. It can be seen that the waveforms of Figure 37 are the only possible solution satisfying all the above as well as the conditions that $i_{CR_1} + i_{CR_2} = i_1$, and that the net area under each diode current curve is zero for each input cycle.

It can be seen that the zero crossings of the output square wave lag the input current by 90°. This is expected since ideally the step recovery diodes are non-linear capacitors.

By reasoning similar to the above, several additional circuit characteristics can be deduced as follows:

1. The only effect of finite but large lifetime is to require more forward area under the current curve than reverse area. This merely reduces the 90° phase lag. The action for extremely long input periods (low frequency) remains to be investigated, but it appears that the circuit should work for lifetimes that are about equal to the input period.
2. Resistive output loading only shifts the phase, as long as a sufficient overdrive current \( i_o \) is used. The peak value of \( i_o \) should not fall below about twice the peak output current.

3. Varying \( V_s \) changes the duty factor of the output without changing the positive and negative voltage excursion. Rise time changes with change of duty cycle occur. In general, rise time depends on the degree of current overdrive due to the inherent clipping action of the circuit. It also depends on the rep rate due to the variation of conduction time and stored charge in the diodes.

4. Changing \( V_1 \) or \( V_2 \) alters the positive or negative excursion, respectively. However, the dc component at \( A \) will remain equal to \( V_o \).

5. Impedance to ground at \( A \) is always approximately zero. Therefore \( R_a \) determines the output impedance.

6. This action is independent of frequency as long as \( i_o \) is of sufficient amplitude.

![Figure 37. Waveforms for Figure 33](image)

The input impedance from the drive side is highly reactive due to inductor \( L_i \), which is necessary from a switching standpoint. This means that a large input current swing and voltage swing both exist. The phase angle is close to 90°, differing from 90° only enough to account for small losses plus the square wave output power. The component of input reactance due to the inductor \( L_i \) can be tuned out by a series capacitor, \( C \), as shown in Figure 38. This allows the source to see only the resistive component of the impedance. Input impedances for this configuration are usually close to 50 ohms.

This circuit is very intolerant of lead inductances, particularly around the loop including \( CR_1, CR_2 \), and the bias sources. Figure 39 illustrates a technique for minimizing these effects using ceramic packaged diodes and metallized ceramic plate capacitors. For this mounting method, the posts on the standard diode packages (Outline 31) have to be machined off.

Areas \( A, B, \) and \( C \) are metallized areas on a high dielectric \( (\varepsilon_r = 10,000) \) ceramic plate which are electrically separated by narrow scratches. The entire back side is metallized. This is sunk flush with the surface of a metal ground plate. A microstrip transmission line board, with full copper ground plane, is butt against the diodes which sit on areas \( A \) and \( B \), such that the board ground plane contacts area \( C \), and the metal plate.

Bias is applied to areas \( A \) and \( B \), and the inductor \( L_i \) is connected to the strap connecting the two diodes. The output is taken from the stripline.

The effective series inductance for diodes mounted this way is \( \approx 400 \mu \text{H} \) per diode. The approximate peak-peak transient ring, stated as a percentage of the output pulse peak amplitude, is estimated to be:

<table>
<thead>
<tr>
<th>( t_{APS} ) (ns)</th>
<th>( P-P ) ring</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>50%</td>
</tr>
<tr>
<td>300</td>
<td>16%</td>
</tr>
<tr>
<td>600</td>
<td>8%</td>
</tr>
</tbody>
</table>

This estimate neglects the effects of ring damping and other effects that can reduce ring, therefore these figures are pessimistic possibly by \( 2:1 \).

d) Unidirectional Impulse Generator: Another useful waveform generator circuit is the Impulse Generator shown in Figure 40. This circuit will convert a sinusoidal input into a train of narrow unidirectional impulses, as shown in Figure 41. The repetition rate of the impulses will be at precisely the frequency of the input. The pulse width can be made extremely narrow, i.e., \( \leq 150 \) ps. The pulse repetition rate can be as low as \( 10 \) MHz. This circuit is useful as a source of narrow, low duty factor video pulses for high speed clock and timing applications. Since the frequency spectrum of a repetitive impulse is a reasonably flat “comb” of discrete frequencies, this circuit is also useful for generating reference frequencies for system testing and for frequency synthesis application. At sufficiently low repetition rates, the circuit can also be useful as a high power wide band noise source. With suitable output structures, this circuit can also be used to generate damped sinusoidal waveforms and as a harmonic frequency multiplier. The operation of the circuit is as follows:

The diode \( CR_1 \) is an SRD whose lifetime \( \tau \) is long compared to the input period of the sinewave, i.e., \( \tau > 10f \_m \).

The bias battery, \( E_b \), when combined with the average diode forward voltage \( V_F \), becomes \( E_b' \) in the equivalent circuit. \( R_c \) is negligibly small, and the peak voltage of \( E_b' \) is
considerably greater than \( E_t' \). During the positive half cycle of the input waveform, the diode is turned on (switch S closed in the equivalent circuit) and charge is stored in it by the positive current. On the negative half cycle, the generator reverses the current through the diode and this charge is removed. The bias voltage is adjusted to make the peak reverse current through the diode a maximum when the last of the stored charge is removed. At this time, the diode stops conducting (S opens) and appears as a capacitor. The resulting rapid cessation of current creates a transient waveform involving \( L, C_{VR} \), and \( R_L \). If \( R_L > \sqrt{L/C_{VR}} \), the transient takes the form of a damped high frequency sinewave of frequency

\[
f_o = \frac{1}{2\pi \sqrt{LC_{VR}}}.
\]

The first half-cycle of this transient forms the output impulse; then the diode becomes forward biased and switch “S” closes again for another cycle. Several observations can be made based on this simple model:

1. The output impulses occur once per input period.
2. The impulse width is \( \pi \sqrt{LC_{VR}^2} \).
3. Since the average value of the output voltage over a cycle must be zero, the impulse height can be related to \( E_t' \) as

\[
V_p = \frac{E_t'TT}{2t_0}.
\]

4. Since the battery \( E_t \) is absorbing energy, it can be replaced by a simple parallel \( R-C \) bias network, which then lets diode recombination current bias the circuit.

This circuit can be easily converted into the following circuits.

**Damped-Waveform Generator**

If a lightly loaded transmission line of \( 1/4 \) wavelength at

\[
\frac{2\pi \sqrt{LC_{VR}}}{1}
\]

the frequency \( 2\pi \sqrt{LC_{VR}} \) is connected across the output of the circuit, as shown in Figure 42, a damped ringing waveform will be produced due to successive reflections on the line.

**Figure 39. Layout of Square Wave Circuit**

**Figure 40. Impulse Generator Circuit**

**Figure 41. Impulse Shunt Generator Typical Current and Voltage Waveforms**

**Figure 42. Damped Waveform Generator**

**Frequency Multiplier**

If the output of the line is then coupled to a resonant circuit or cavity at the output frequency, an efficient frequency multiplier is the result.
4. Miscellaneous Pulse and Digital Circuits

The SRD and the various basic SRD circuits described previously can be used as building blocks, with some modification, to achieve a large variety of digital and analog functions. Some of these are described in this section.

a) Variable Pulse Delay Generator: If a constant-amplitude pulse is applied to a shunt SRD circuit as in Figure 13, the leading edge will be delayed by the storage time of the SRD and sharpened by the fast transition of the diode. In the usual application, \( I_F \) remains constant and the rise time sharpening action of the circuit is taken advantage of. If in addition, \( I_F \) is made variable with time, the result will be modulation of the delay time to the start of the output pulse. Delays from a few picoseconds to over 100 nanoseconds are possible. If the input pulse has stable amplitude, the time jitter associated with this type of operation will be very small, typically less than a few picoseconds for a delay of 10 ns.

The delay modulation bandwidth (to the 3 dB point) of such a circuit is limited by diode lifetime \( \tau \) to:

\[
\omega_m = \frac{1}{2\pi \tau}
\]

For delays of 10 ns and less this circuit has great advantages over the conventional voltage ramp circuit shown in Figure 43. These are listed below.

1. In a typical voltage-ramp delay circuit there is always a finite inductance in series with the ramp capacitor. When very small capacitors are used for short delays, a resonance or ringing effect exists, causing the ramp to have a considerable ripple. If the peak slope of this ripple exceeds the ramp slope, the ramp will not be monotonic, and delay jumps are possible. If the ripple is smaller than this critical value, the delay vs. bias relation will be lumpy.

In an SRD charge ramp circuit, the SRD is so low in impedance that no resonance is possible during the ramp. A series resistor can be used to damp any possible ringing without affecting the constant current reverse pulse source. Any remaining ripple in reverse current is integrated out further by the absolute charge sensitivity of the SRD (it snaps at zero charge, independent of inductive lead voltage drops).

2. A voltage-ramp delay circuit requires some type of voltage sensitive pick-off element, which can have noise or ripple causing a jitter in the pick-off time. To minimize jitter, ramps have to be quite steep. This requires use of small capacitors (which make the resonances worse) and bigger voltage swings (which cause non-linearities in delay vs. pick-off voltage).

An SRD charge-ramp delay circuit automatically provides a very sharp (< 1 ns) rise time output as the charge reaches zero, with no additional time jitter from pick-off circuits.

3. Due to elimination of pick-off circuitry and absence of the need for high impedance ramp current sources, the circuitry of an SRD charge ramp delay function is much simpler than for an R-C ramp plus pick-off circuit.

b) High Speed SRD-DTL NOR Gate: The controlled charge storage of an SRD makes it useful as a voltage offset diode for fast logic gates. In Figure 44, if \( CR_1 \) is an ideal diode, turnoff of transistor \( Q_2 \) is very slow since its base charge must leak to ground through resistor \( R_2 \) at a slow rate. If \( CR_1 \) is an SRD whose lifetime is equal to the transistor base lifetime, collector current of \( Q_1 \) can extract base current from \( Q_2 \) at a high rate, drastically reducing delay of the gate.

The proper operation of this circuit requires that \( CR_1 \) store at least as much charge as the transistor at the current level used. Once this charge is determined, the SRD lifetime \( \tau \) can be chosen from the relation

\[
\tau_{min} = \frac{Q_s}{I_F}
\]

where

\( Q_s \) = required stored charge

\( I_F \) = transistor base current and SRD forward current
c) Wide Band Pulse Counting FM Discriminator: The circuit of Figure 45 will convert a train of pulses of varying amplitude into a train of pulses of constant areas. The time average of the output pulses will be proportional to the input frequency and independent of the input amplitude. Being a true pulse-counting discriminator, this circuit is particularly suitable as a wide band FM discriminator with bandwidth on the order of 1 MHz for a single diode circuit.

Where

\[ i_p = \text{Peak RF current} \]
\[ f = \text{RF frequency} \]
\[ Q = \text{Charge} \]

The bias current \( I_f \) required to cause full cycle conduction is:

\[ I_f = \frac{Q}{\tau} \frac{i_p}{\pi f \tau} \]

And the current gain,

\[ \frac{i_p}{I_f} = \frac{\pi f \tau}{i_p} \]

If two HP 5082-0202 diodes are used at a frequency of 200 MHz, and a diode lifetime of 200 nsec (typical HP 5082-0202),

\[ \text{gain} = \pi \left(200 \times 10^6\right) \left(200 \times 10^{-9}\right) = 126 \]

Harmonic generation due to the fast diode transition is considerable, but can be suppressed with filters.

Such a circuit would be very suitable as an amplitude control element in a high frequency RF to DC power converter. A basic scheme for such a power converter is shown in Figure 47.

d) Amplitude-Controlled RF-DC Converter: By varying the bias current in the circuit of Figure 46, the RF conduction angle can be varied in a manner analogous to phase control of 60 Hz power by SCR's. This process is basically conservative with almost no energy lost in the diodes, so a relatively large RF power can be controlled safely with a low power diode.

The charge displaced in 1/2 RF cycle is

\[ Q = \int_0^\pi i \, dt = \frac{i_p}{\pi f} \]

e) One-Shot Voltage Impulse Generator: This circuit is a unique application of the SRD together with a shorted transmission line in which a single isolated transient is set up on the line without the need of any terminating resistors to suppress re-reflections on the line from either the source or the shorted end.
In some applications, it is necessary to develop a very narrow voltage impulse across a high impedance load. This can be done with one SRD driving a shorted transmission line. The load is connected at an appropriate distance from the shorted end of the line for the pulse width desired, as shown in Figure 48.

![Figure 48. Conventional Narrow-Pulse Circuit](image)

When the SRD releases a step of current, this step propagates down the line to the short, producing a step of voltage across $R_L$. At the short, the step voltage reverses polarity and reflects back toward the source, causing the load voltage to return to zero as it passes $R_L$ on its return trip. It then is absorbed in the resistive pad at the source, to prevent re-reflection and resultant multiple pulses. This scheme suffers from the 6 dB amplitude loss of the attenuator which is necessary to give a resistive source impedance. Another scheme, which eliminates the attenuator and therefore gives 6 dB more output without serious re-reflection, is shown in Figure 49. Its operation is best understood by studying waveforms on a shorted line with a source resistance equal to $Z_o$, as shown in Figure 50.

![Figure 49. Improved Single-Pulse Circuit](image)

Initially, half the source pulse current flows into the $Z_o$ termination and half into the $Z_o$, surge impedance of the line. A positive waveform travels to the short, reflects 100% negative, and travels back to the source, wiping out all line voltage as it returns. The line current doubles as the return reflection passes each point on the line.

Notice in Figure 50 that the sending end voltage returned just to zero, due to the action of the resistor $R_1$ on the traveling wave. If $R_1$ were not there, the sending end voltage $V_s$ would have jumped to $-iZ_d/2$ on the return of the traveling wave, and a new reflection would be sent out.

![Figure 50. Resistive Source Waveforms](image)

The fact that $R_1$ allows the $V_s$ to just return to zero suggests that a diode and a small bias battery might be substituted for $R_1$ with the same result, a complete absorption of the traveling wave from the short. This turns out to be the case. The SRD of Figure 49, together with a capacitor $C_1$, clips the returning wave at zero and absorbs the difference between the source current and the total line current, and completely stops the transient. This is possible because the SRD has a very fast forward turn-on.

An SRD will act as an almost perfect waveform clipping diode for a waveform as fast as its own transition time. Thus a 100 ps transition time diode will turn on from back bias with very small overshoot in response to a 100 ps rise time
forward current waveform. This property of the SRD is often overlooked. Because the SRD exhibits charge storage, it is usually unnecessarily mentally excluded from use in high speed switching applications.

An energy equal to \( \frac{1}{2} L \left( \frac{d}{2} \right)^2 \) is stored on the line, where \( L = Z_{0} \) is the low frequency inductance of the line, and \( i \) is the source current step amplitude (\( i \) is the one-way time delay of the line length). This energy is eventually slowly absorbed in SRD series resistance and slight charging of capacitor \( C \), and for all practical purposes only one pulse appears across \( R_{S} \), and this is not attenuated by any 6 dB pad.

This whole argument has been based on a tacit assumption of zero rise time steps. If a finite rise time step is applied to a diode-terminated line of this type, the impedance is too high over most of the transient, and a considerable positive voltage reflection will occur. However, the inclusion of the optimum value of shunt diode junction capacitance will remove most of the reflection. It has been calculated and experimentally shown that the capacitance present in an SRD, which gives a certain rise time pulse, is close to the optimum value required for a perfect termination for a reflection which has the same rise time. Because of this, the circuit of Figure 49 is effective even for steps of finite rise time.

5. Special Topics

This section outlines some techniques and design approaches which are of general interest when working with high speed pulse circuits. The practical realization of these circuits demands practices that are more stringent than those in microwave circuits because the bandwidths involved are extremely broad and often extend from GHz to dc.

a) Diode Mounting for Pulse Applications: In practice it is very difficult to construct lumped circuits without excessively large stray reactances, especially for rise times below 0.2 ns and impedance levels below 50 ohms.

For rise times around 100 ps, a transmission line mounting for the SRD is by far the easiest and best method. The three common methods and the surge impedance which the diode “faces” in each case are shown in Figure 51.

![Figure 51. Line Mounting for SRD's](image)

The end mounting is seldom used, since only one output is available and traveling-wave time separation must be used to separate the fast output waveform from the drive waveform. The series connection is occasionally used to form a fast trailing edge on a pulse traveling down the line.

The shunt mounting is by far the commonest, and is very useful as a step sharpener. Micro- stripline is preferable to coax for shunt mounting, since the mutual inductance of packaged diodes has typically half the value in microstrip that it has in coax.

Even if the drive circuitry for the SRD sharpener is far from a \( Z_{0} \) match to the line, a very good pulse leading edge can be produced by a line-mounted diode, since it takes some time for a traveling wave to reach the source from the diode and for the reflection to return, and the pulse will be clean at least for this amount of time. In addition, lumped-circuit effects of the diode and the driving circuitry are not allowed to combine directly, so the pulse reflection from a poorly matched source will often be less serious than the perturbation caused by direct connection of the source and the SRD.

b) Effect of Parasitics on Overshoot and Ringing: Calculation of the exact leading edge shape is much easier with a properly line-mounted diode, since the line is known to be resistive for a certain amount of time (the round-trip time for a wave at the speed of light in the line’s medium to reach the first discontinuity and return).

For a shunt-mounted diode, the equivalent circuit affecting the leading edge shape is shown in Figure 52.

![Figure 52. Shunt Mount Diode-Equivalent Circuit](image)

Assuming that the diode switches instantaneously, the leading edge of the waveform will be of the form:

\[
E_{d}(S) = I_{g} \frac{Z_{0}}{2} \left( \frac{1}{S^{2} + S \frac{Z_{n}}{2L_{s}} + \frac{1}{L_{s}C_{VR}}} \right)
\]

where

- \( \omega_{n} = \) ringing frequency
- \( \zeta = \) damping factor

and \( \omega_{n} = \frac{1}{L_{s}C_{VR}}, \zeta = \frac{Z_{0} \sqrt{C_{VR}}}{4 \sqrt{L_{s}}} \)

This waveform is shown in Figure 53 for various values of the damping factor \( \zeta \). Knowing the circuit constants, the peak overshoot and the approximate ringing frequency can be obtained from this figure. Actual measured overshoot will be less if the diode’s \( t_{r} \) is not much less than \( 1/\omega_{n} \).
Figure 53. Transient Responses of Figure 52

When $\zeta < 2$, the rise time from Figure 53 will be less than that calculated on a straight R-C basis. For these cases, use Figure 53 rather than an R-C calculation.

c) Charge Insertion Methods: There are many methods of getting the required stored charge into a SRD, one of which is the dc bias used in the step waveform sharpener. Referring back to Equation 1,

$$i(t) = \frac{dQ}{dt} + \frac{Q}{\tau} \quad \text{for} \quad Q > 0$$

where

- $i =$ total instantaneous diode current
- $Q =$ charge stored at junction
- $\tau =$ minority carrier lifetime of diode

Taking Laplace transforms and solving for $Q(s)$

$$Q(s) = \frac{\tau i(s)}{1 + s\tau}$$

The time waveforms of $Q(t)$ corresponding to a few selected time functions for $i(t)$ are shown in Figure 54.

It can be seen that a constant forward current is a very slow way to build up charge. An impulse of current (or its equivalent step of charge) is the quickest way, but recombination causes the stored charge to decay.

To quickly build up to a steady value of charge, an impulse followed by a dc step is appropriate. These special forward-current drive waveforms are useful for pulse circuits which must operate from very low repetition rates to very high ones (the impulse plus step is good for both extremes of repetition rate), although a price must be paid in terms of circuit complexity to produce special forward current waveforms.

Figure 54(d) shows the charge-time waveforms possible with sinusoidal current drive for two extreme conditions: one where the drive waveform period $T$ is much greater than diode lifetime, and one where $T$ is much less than lifetime. The former case corresponds to the case present in a typical ac rectifier, where stored charge is instantaneously proportional to current. The latter case is one for which the charge barely reaches zero, and no rectification or switching occurs. Most practical cases fall between these limits, and switching occurs somewhere in the cycle.

Figure 54. $Q(t)$ for typical $i(t)$

It has been experimentally shown that the charge insertion method used has no measurable effect on the transition characteristics of an SRD. The published dynamic characteristics measured using dc bias are completely valid provided the charge present at the start of the storage interval is used as the basis of comparison.

REFERENCES


2. HP Application Note 920.

BIBLIOGRAPHY


