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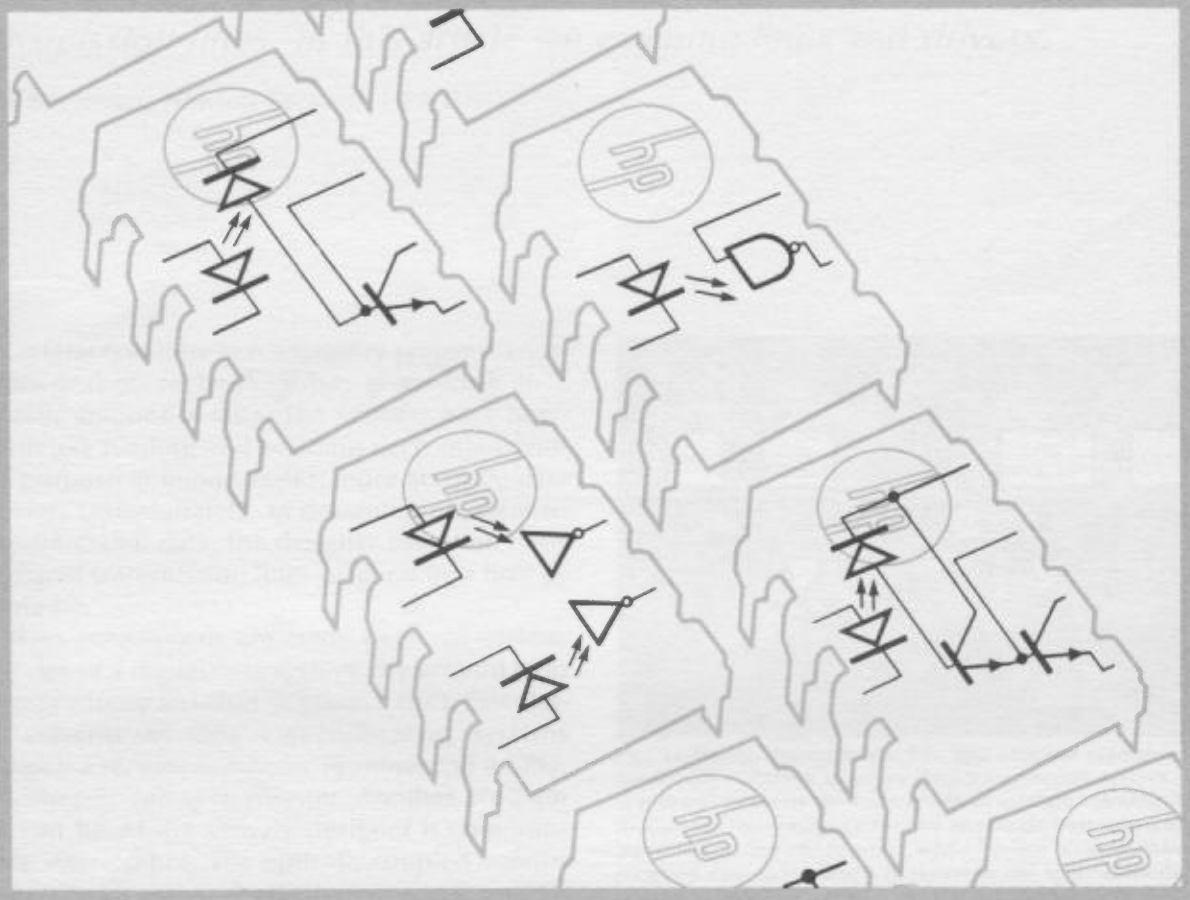

Digital Data Transmission Using Optically Coupled Isolators

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Designer's Guide to: Optoisolators—Part 1

Optically coupled isolators are extremely versatile in digital data transmission lines. In this article we examine lines and drivers.

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The interaction between telemetry systems, computers and IC technology has given birth to a fantastic amount of data. The systems have been alternately feeding and needing each other with one purpose in mind—faster, more accurate data transfer. Unfortunately, in designing a system to transmit digital data, the designer too often finds his digital transmission lines plagued by a host of problems.

When connections are made between various modules of a digital data system, the ground loop often produces an offset or ground shift. Circulating currents in data communication systems between a remote computer terminal and a CPU, for example, can spell disaster. Another problem that can haunt the unwary designer is common-mode interference. The optically coupled isolator (OCI) offers a convenient, effective and economical solution to both of these problems.

Indeed, the advantages of OCI's are truly impressive: Unlike transformers, OCI's can hold a given logic state indefinitely; unlike relays, they have high data rate capability (dc to beyond 10 M-bits/sec); and unlike differential-amplifier data receptors, OCI's can tolerate high common-mode voltages (up to 2500V). The OCI has no inductive coupling, has small capacitive coupling, generates no EMI and has no mechanical contacts. Furthermore, it can withstand shock and vibration, requires little power and is IC-compatible.

Optical couplers electrically isolate two circuits, yet permit the transfer of data through a transparent insulation. On the input side of an OCI, a LED or IRED emits photons; on the receiving side, a photodetector (phototransistor or PIN photodiode) converts the optical signal to an electrical signal by switching the detector.

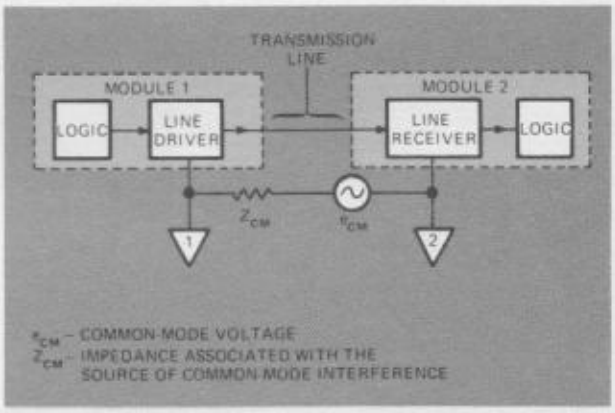


Fig. 1—Driver, transmission line and receiver comprise the functional elements of every data transmission system. The line driver converts the logic levels of Module 1 (transmitting module) to the configuration and amplitude best suited to the transmission line and receiver, while the line receiver converts received data to the levels required by the logic in Module 2 (receiving module).

Our tutorial, 4-part Designer's Guide series will center on drivers, lines and receivers. This article will explore drivers and transmission lines, while the second will cover passive terminations. Active terminations and enhancement of common-mode rejection are the subject of the third article, with the fourth installment centering on data rate enhancement and multiplex applications.

Rather than restricting our discussion to performance obtainable with particular circuits, we will emphasize broadly applicable design principles and circuit analysis. By referring to data sheets, you can then apply the principles presented to different OCI's in other circuits.

It takes three to communicate

Three functional elements (**Fig. 1**) exist in every digital data system: a line driver, the transmission line and a line receiver.

A line driver accepts as its input the logic levels developed in the transmitting module (Module 1 in **Fig. 1**) and converts them to a form that is compatible with the transmission line and line receiver. The transmission line simply connects the line driver to the line receiver, but its characteristics can profoundly influence system performance with regard to bandwidth, common-mode rejection and compatibility with the line driver. At the opposite end of the transmission line, the line receiver responds to the signals delivered through the line and converts them to be compatible with the logic levels required in the receiving module (Module 2).

As far as establishing error-free performance, the receiver is typically the most important element of the system; and it is in the design of line receivers where optoisolators are usually found. For this reason, most of this series will deal with making the optoisolator input and output compatible, respectively, with the driver/line and the receiver module logic levels. Let's consider the line driver first.

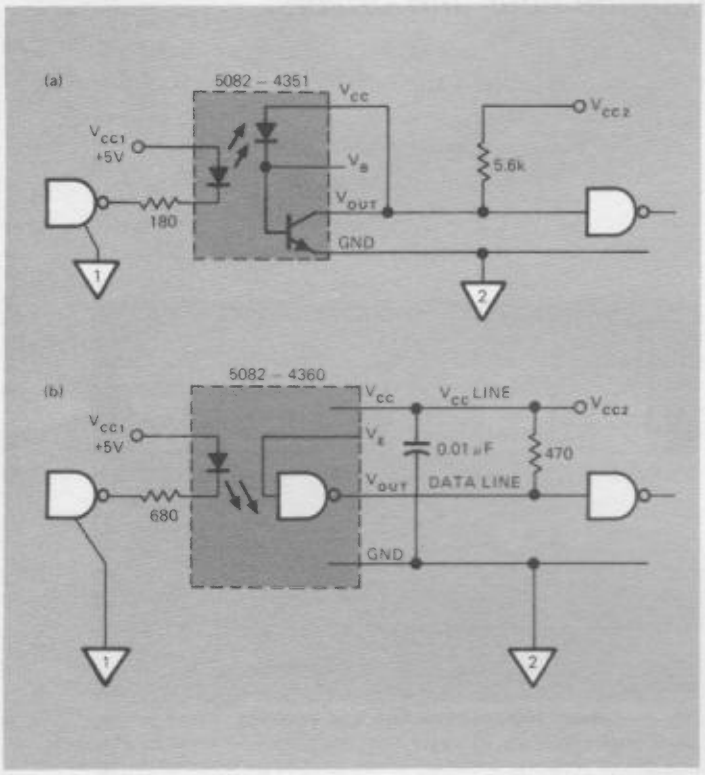


Fig. 2—Opto-isolators can function as line drivers. Using one as a 2-terminal switch (**a**) is the direct approach, but it suffers from greater noise interference due to low line current. You can achieve higher line current and data rates by carrying Module 2's supply voltage back to Module 1 through a third line (**b**).

Put an OCI in the driver's seat

Transmission lines and line receivers require line drivers that produce signals of the optimum configuration and amplitude. Briefly, configuration considerations include current/voltage sourcing or sinking, balanced or single-ended system, and polarity reversing or nonreversing. Amplitude consideration, on the other hand, takes into account current or voltage threshold requirements at the receiver, impedance of the transmission line and interference amplitude (the latter being especially important in single-ended systems).

Current or voltage sinking. For systems requiring such a configuration, the optoisolator can serve as the line driver. Some types of OCI's have outputs that can function as simple 2-terminal switches, as shown in **Fig. 2a.** However, because the current flowing in the line is relatively low, the system is more vulnerable to interference than it would be if higher line current was used. To obtain higher line current and data rate, an optoisolator could still be used, but the system would then require an additional wire to bring V_{CC2} from Module 2 to power the amplifier in the output of the optoisolator (**Fig. 2b**). You could

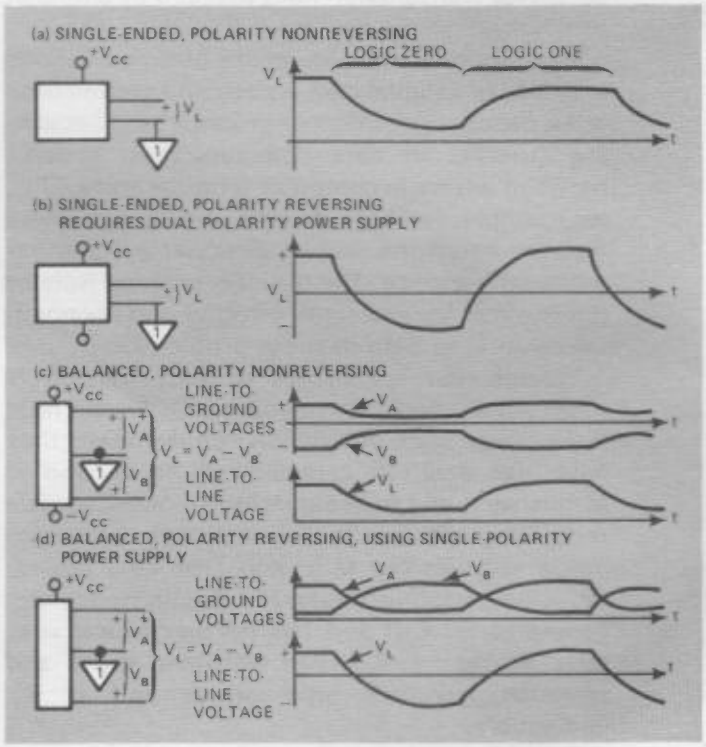


Fig. 3—Both single-ended or balanced drivers can be either polarity nonreversing or polarity reversing. Balanced systems (**c** and **d**) are generally preferred because receiver common-mode rejection subtracts out the common line noise. As a result, balanced systems provide greater common-mode rejection for given line currents.

obtain still higher line current, but a lower data rate, by using a high gain optoisolator such as the 5082-4370/71 instead of the 5082-4360.

Current or voltage sourcing line drivers (conventional types) are the most commonly used, mainly because they provide higher line currents than is possible with optoisolator inputs. We will say more about them later.

Balanced or single ended. With 2-conductor transmission lines (either coax or unshielded twisted pair), the driver may be either single-ended or differential. A balanced system requires a differential line driver and is often preferred because it offers higher immunity to electromagnetically induced interference (EMI) by causing the interference to appear in common mode, while the desired signal is differential mode.

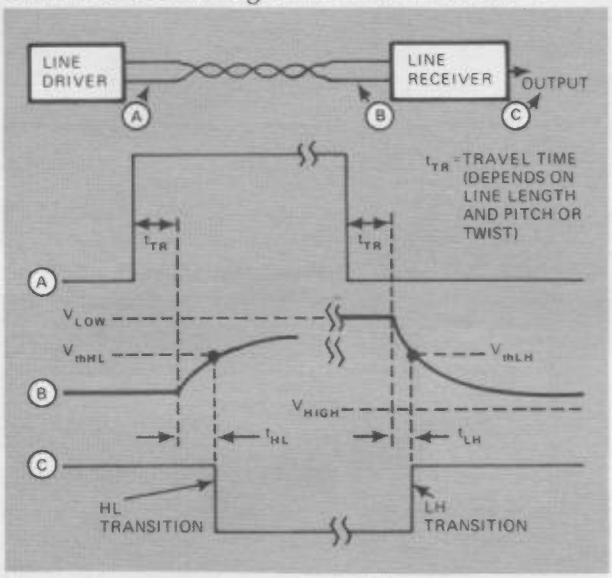


Fig. 4—A square pulse generated at line drive (A) possesses steel edges that are exponentially rounded by the skin-effect and dielectric losses of the transmission line. Since the line receiver switches at a threshold V_{th}, the line introduces a delay time (transit time t_{TR} plus rise time t_{HL}) as seen in **B**. After time $t_{TR} + t_{HL}$ has elapsed the receiver makes a HIGH-to-LOW (HL) transition. On the trailing edge of the pulse, the reverse takes place

Polarity reversing or nonreversing. Both balanced and single-ended systems may be operated with either polarity reversing or polarity nonreversing signals. In a single-ended system, one side is usually connected to Ground 1 (of Module 1) and the line voltage appearing in response to changes in the logic state can be seen in **Figs. 3a** and **3b.**

For balanced systems, the voltage on each line can be referred to Ground 1. But what is significant in this case is the line-to-line voltage, since a conductor carrying Ground 1 is not necessarily brought to the receiving end. The line-to-ground and line-to-line voltages for balanced systems under varying logic states appear in **Figs. 3c** and **3d.**

Amplitude considerations for line drivers should take account of the current (or voltage) required by the line receiver. Obviously, optoisolators cannot be operated unless the line voltage (V_L) exceeds the operating voltage of the terminating circuit. Operating voltage can vary from as little as 1.5V (V_F of the optoisolator's input diode) to as much as 2.4V for an active termination.

The characteristic impedance of the transmission line affects amplitude considerations. Low impedance lines, such as coaxial, require a fairly large current drive capability to develop the voltage required by the line receiver.

Finally, there's the matter of noise. Ideally, the desired signal is carried at voltages and currents much larger than the noise amplitude. By designing the threshold of the line receiver to respond only to the high amplitudes produced by the desired signal, the lower amplitude of the interference becomes quite insignificant. The need for high amplitude signals will prove greater in single-ended than in balanced systems. This is so because in balanced systems interference is coupled with equal phase and amplitude into both sides and can be easily subtracted out in a differential receiver.

Amplitude balancing is desirable for data rate optimization. That is, with respect to the logic transition threshold, the asymptote for a HIGH should exceed the LOW-to-HIGH (LH) threshold to the same extent that the LOW asymptote exceeds the HIGH-to-LOW (HL) threshold (**Fig. 4**).

Note the inversion

Referring to **Fig. 4,** have you noticed what appears at first to be a polarity discrepancy between waveforms and nomenclature in this figure and others? Obviously it is not, since it stems from the standard specification of optoisolator propagation delay. For example, t_{PHL} is the propagation delay for a HIGH-to-LOW transition at the output of the optoisolator. In most applications with the most commonly used types of optoisolators, a LOW output requires a HIGH input voltage (or current), taking the forward voltage (and current) of the input diode as positive. Thus, an HL delay is associated with a rising input voltage.

Table 1 lists TTL and MOS line drivers suitable for lines terminated with OCI's. Other line drivers can be constructed from discrete components. Keep in mind that because line receivers using OCI's have high thresholds, you should use drivers with nonreversing output polarities and with amplitude characters such that logic ONE and logic ZERO line voltages deviate equidistantly

TYPE NO.	INPUT SIGNAL	POWER SUPPLY	OUTPUT CHARACTERISTICS "HIGH" STATE	OUTPUT CHARACTERISTICS "LOW" STATE	COMMENTS	TYPICAL APPLICATION
			FOR HIGH DATA RATES – TO 15M bit/sec			
DM 8830 μA 9614	TTL TTL	+5V +5V	LOW-Z SOURCE 40 mA, +3V	LOW-Z SINK 120 mA, +0.5V	BOTH HAVE INTERNAL PHASE SPLITTER; 9614 HAS SEPARABLE SOURCE/SINK	TWISTED PAIR SHIELDED DIFFERENTIAL–POLARITY REVERSING
μA 9621	TTL	+5V TO +14V	LOW-Z OR 130Ω E_g = 2.5 TO 11.5V	LOW-Z OR 130Ω $E_o \approx 0$	INTERNAL RES. AVAILABLE FOR BACKMATCH TYP. TWISTED PAIR, UNSHIELDED	TWISTED PAIR, UNSHIELDED DIFFERENTIAL–POLARITY REVERSING
LM 75324 75325	TTL TTL	+5 TO 17V +5 TO 24V	400 mA SOURCE 600 mA SOURCE	400 mA SINK 600 mA SINK	MEMORY DRIVERS–BOTH NEED EXTERNAL PHASE SPLITTER FOR DIFFERENTIAL OUTPUT	EXTERNAL BACK MATCH, DIFFERENTIAL–REVERSING OR NONREVERSING
75451 75452 75453 75454	TTL TTL TTL TTL	+5V +5V +5V +5V	OPEN COLLECTOR $V_{CEO} > 30V$	SINK 300 mA	NAND, AND, NOR, OR } FOR DIFFERENTIAL OPERATION NEED EXTERNAL PHASE SPLITTER UNLESS USED IN OR/NOR OR AND/NAND PAIRS	EXTERNAL BACK MATCH. DIFFERENTIAL–REVERSING OR NONREVERSING
			FOR MEDIUM DATA RATES – TO 1 Mbit/sec			
MC 75113	TTL	+5V, –6V	SOURCE/SINK 20 mA	SOURCE/SINK OPEN	CURRENT-SOURCE FOR HI-Z_0 LINES	DIFFERENTIAL–NONREVERSING
75491	MOS	UP TO +10V	SOURCE 50 mA OPEN COLLECTOR	OPEN EMITTER SINK 50 mA	QUAD LED DRIVER–w/ EXTERNAL PHASE SPLITTER CAN BE DIFFERENTIAL LINE DRIVER	SINGLE-END QUAD OR DUAL DIFFERENTIAL DRIVER
75492	MOS	UP TO +10V	OPEN COLLECTOR	SINK 250 mA	HEX LED DRIVER–w/ EXTERNAL PHASE SPLITTER & PULL-UP RESISTOR MAKES LINE DRIVER	SINGLE-END HEX OR TRIPLE DIFFERENTIAL DRIVER
			FOR LOW DATA RATES – TO 50k bit/sec			
MC 1488 μA 9616	TTL	+9, –9	+5V, 300Ω	–6V, 300Ω	QUAD, TRIPLE } BOTH HAVE 10 mA LIMITER 9616 HAS "INHIBIT" INPUTS	RS-232-C UNBALANCED, POLARITY–REVERSING
75109 75110	TTL	+5, –5	OFF	3.5-7.0 mA SINK 6.5-15 mA SINK	INTERNAL PHASE SPLIT; NEED EXTERNAL PULL-UP RESISTOR; CURRENT LIMIT OUTPUT	DIFFERENTIAL–POLARITY–REVERSING

Table 1—Integrated drivers for lines terminated with optoisolators.

above and below the threshold voltage. Drivers with polarity reversing output need only have enough amplitude to exceed the threshold with either polarity; balancing is then achieved by using a pair of OCI's operating in a balanced, split-phase circuit. This technique will be discussed in detail later.

Impedance Considerations. Where the possibility exists of high EMI, you should make the driver output impedance to Ground 1 either low with respect to the characteristic impedance of the line, or balanced with respect to Ground 1. With this advice, we come to the second element of the data transmission system—the transmission line itself.

Meanwhile, on down the line. . . .

In choosing a cable for data transmission, you should consider four factors: the characteristic impedance (Z_0, in ohms), the dc resistance of line (R_W, in ohms per unit length), bandwidth or data rate capability and effectiveness against common-mode interference. Of course, there are also the usual considerations of cost, availability, ruggedness, size, and so forth. But these are not areas of concern since they do not directly affect performance (except for cost and size).

Characteristic Impedance (Z_0) becomes an important consideration only when low loss cable is used in a high speed system with distances less than 50 meters. As a rule, coaxial cables have the lowest characteristic impedance, followed by shielded twisted pair, then by unshielded twisted pair. The characteristic impedance of these cables remains the same regardless of the length, while dc resistance is proportional to length.

If the characteristic impedance is not listed by the manufacturer, you can measure it easily by

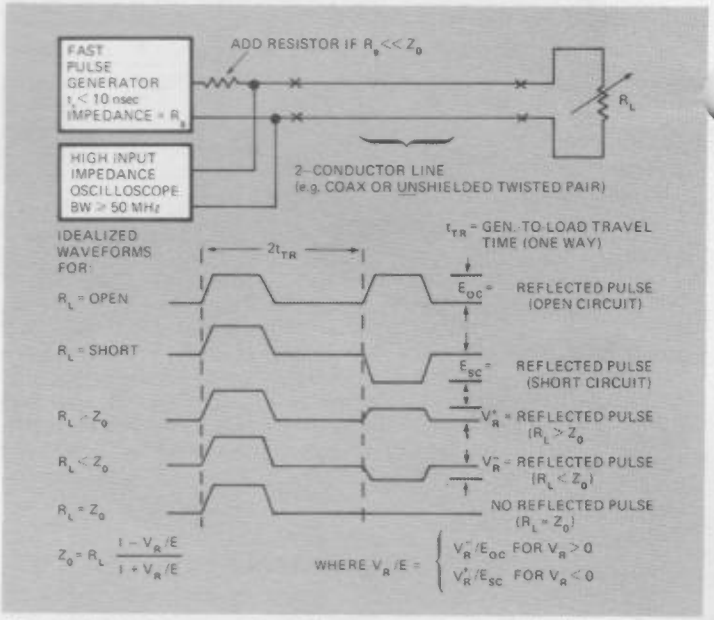


Fig. 5—In the time domain reflectometry (TDR) method for measuring characteristic impedance (Z_0) of a 2-conductor transmission line (single-ended or balanced unshielded line), both the waveform of the generated pulse and its reflection appear on the scope, separated by twice the transit time. Only one value of R_L need be used in the measurements provided $R_L \neq Z_0$.

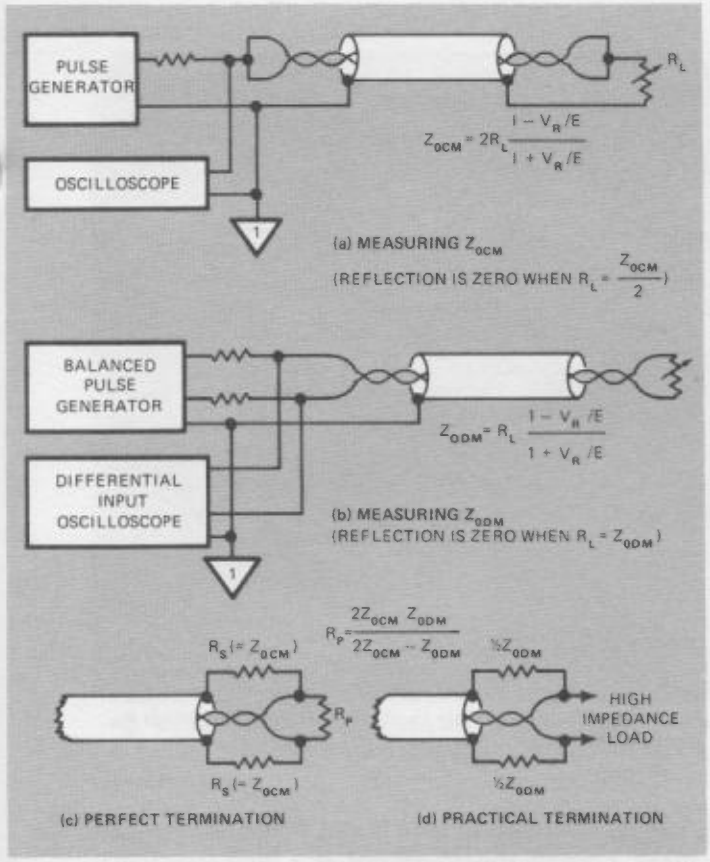


Fig. 6—To measure common-mode (Z_{0CM}) and differential-mode (Z_{0DM}) characteristic impedance of a shielded twisted pair, use the TDR method and circuits of **a** and **b.** Then calculate Z_{0CM} and Z_{0DM} and use this information, in turn, to design a perfect (**c**) or practical (**d**) termination. Perfect terminations absorb all incident energy from the driver and line, while practical terminations reflect back an insignificant amount.

the time domain reflectometry (TDR) method (**Fig. 5**). Set the pulse duration short enough to permit observation of the baseline as well as the reflection. On the other hand, the sweep time must be greater than $2t_{TR}$, the travel time for the pulse edge to go from scope to load and back. Keep in mind that propagation velocity for coaxial cable is less than 0.3 m/nsec while for twisted pair lines, the velocity may be much slower, depending on the pitch of the twist. At a velocity of 0.2 m/nsec, a cable of 10 meters will have a round trip time ($2t_{TR}$) of 100 nsec.

Twist it, shield it—and you get two

Shielded twisted pair line, because of the shield, has two characteristic impedances: common mode (Z_{0CM}) and differential mode Z_{0DM}). Once again, you can use TDR techniques to measure these impedances, with the circuits of **Fig. 6** and the pulse generator, oscilloscope and waveforms of **Fig. 5.** Notice, however, that the measurements do not directly yield the resistor value to be used in the termination. Rather, they are used as in **Fig. 6** to compute the resistance values needed for a perfect termination. Common-mode signals are terminated with $R_S = Z_{0CM}$ from each line to ground (shield). Differential-mode signals are terminated with Z_{0DM} from line to line, so R_P in parallel with $2Z_{0CM}$ provides a net line-to-line resistance of Z_{0DM}.

$$R_P = (2Z_{0CM}\, Z_{0DM})/(2Z_{0CM} - Z_{0DM}) \qquad (1)$$

Because of parasitic impedances in the apparatus, the waveforms you observe in TDR may not be as clean as those represented in **Fig. 5.** To obtain accurate information, we recommend that you perform the TDR measurement for several values of R_L, selected so that some of them cause positive reflections and others negative. Then take as Z_0 the average obtained by calculating Z_0 for each observation according to:

$$Z_0 = R_L(1 - V_R/|E|)/(1 + V_R/|E|) \qquad (2)$$

Here V_R is the reflected pulse when R_L is connected, while E is the reflected pulse when the line is open (for $R_L > Z_0$) or shorted (for $R_L < Z_0$).

DC resistance (R_W) of the line is important to the extent that it limits the dc current available at the termination. Note that the total line resistance to be considered is the "loop resistance" encountered as current flows to and from the load. It shows up at the termination as part of the source internal resistance; the remainder is the internal resistance of the line driver. For designing a resistive termination, this internal resistance information can be represented either as a "source line" for graphical solutions or as a Thevenin or Norton Equivalent circuit. You obtain the data in a dc (not pulsed) measurement (**Fig. 7**).

Bandwidth, or data rate capability, of the transmission line is affected by the line's resistance. But other loss factors also affect the transient response. The waveforms of **Fig. 4** illustrate the delay in response to step transient signals. (Travel or transit time is not included as part of the logic delay because it is the same for both HL or LH transitions.)

The amplitude of the line driver output and the threshold of the line receiver can affect the logic delay. For this reason, although the transmission line affects the data rate capability, a data rate figure cannot be stated for the cable alone unless the threshold of the line receiver is exactly halfway between the HIGH-state and LOW-state levels. And even if $V_{thLH} = V_{thHL} = (V_{HIGH} + V_{LOW})/2$, the delay can be distorted if the time between logic changes is less than that required for the transient to reach steady state at V_{HIGH} or V_{LOW}. At any rate, it is worthwhile examining the

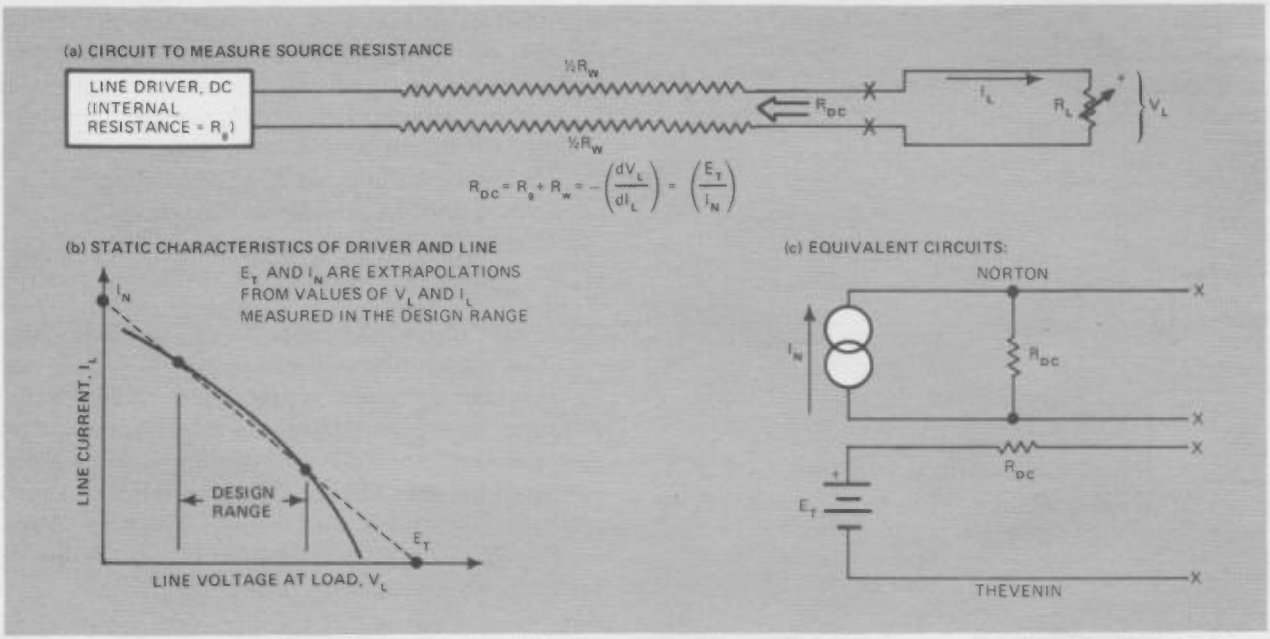


Fig. 7—To obtain the dc resistance looking backward into the line (**a**) from the termination, vary R_L and plot line current vs. line voltage (**b**). Extrapolate to obtain I_N and E_T. This yields R_{DC}, from which you can draw the dc equivalent circuit (**c**).

effects of cable properties on logic delay.

Attenuation of a line depends on frequency and the length and quality of the line. **Fig. 8** illustrates some typical attenuation characteristics.

Notice that the curves have a slope of "one-half," that is, α_0 changes by $\sqrt{10}$, or half a decade per decade of frequency. While this relationship doesn't hold for all types of cable, it is based on the theoretical analysis of skin effect and has been substantially verified by measurements.

So, if attenuation data is not available, you can make a single measurement at a high frequency and use it to provide a curve of α_0 vs. frequency. With this information and the curve in **Fig. 9,** you can then compute the values of t_{PHL} and t_{PLH} if the line length, line driver amplitude, and line receiver thresholds are known.

Measuring attenuation step by step

To measure the attenuation characteristic (α_0)

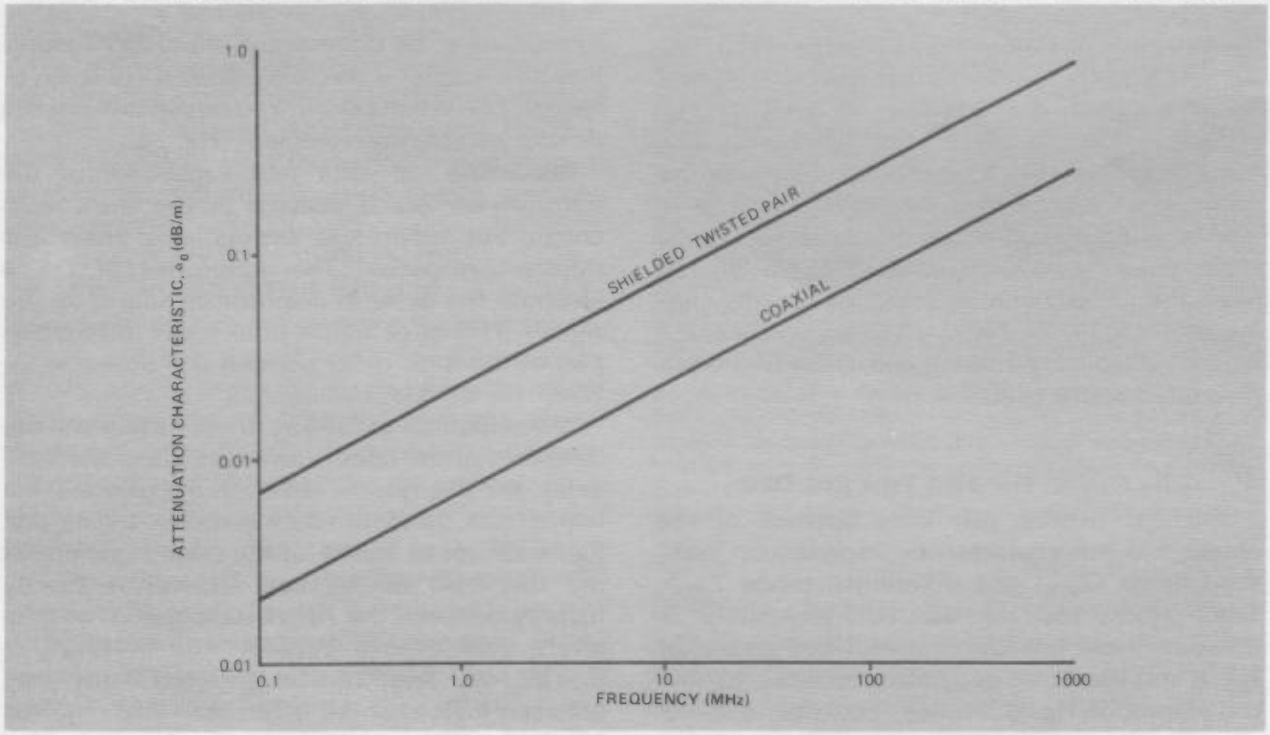


Fig. 8—Transmission line attenuation as a function of frequency graph can be used to obtain f_o, which is then used to calculate the delay time (see example).

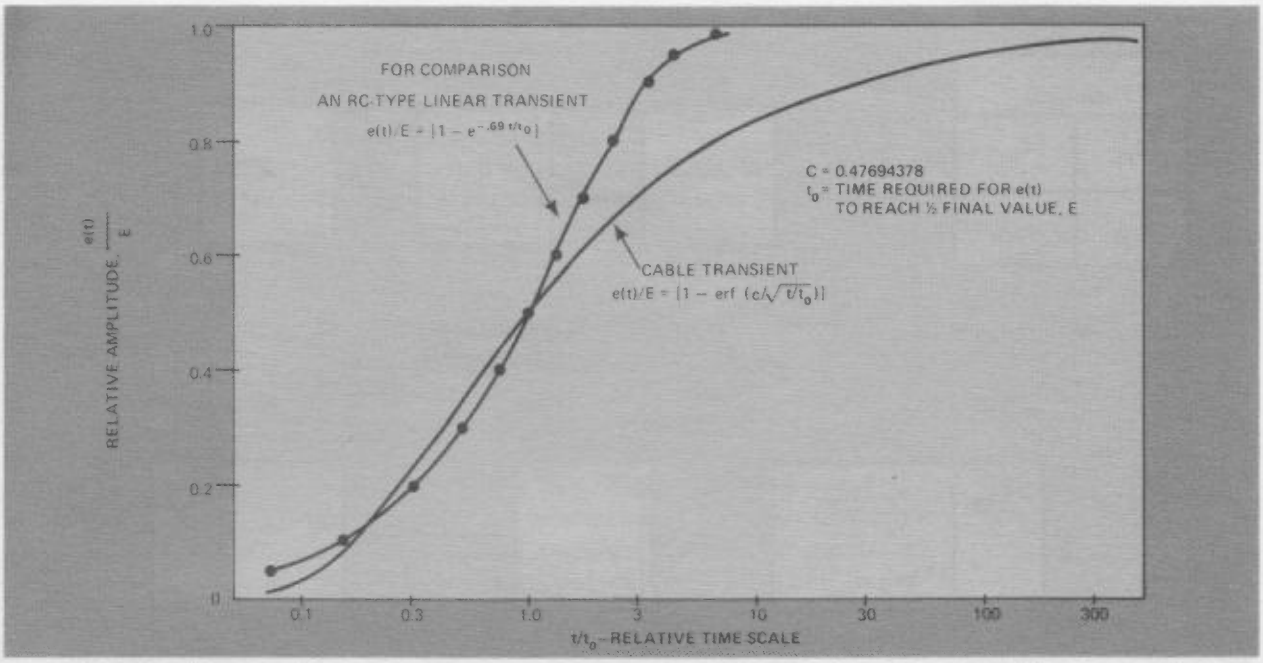


Fig. 9—Normalized transmission line response curve to a step change, E obtains the cable-imposed HL or LH delay when switching thresholds and asymptotic levels are applied. This curve is used to obtain t/t_0 in claculating the delay time (see example).

for a particular sample of transmission line:

1. Measure the characteristic impedance (Z_0) of the transmission line as explained earlier,
2. Set a signal generator to some convenient frequency (f_0) and select a convenient amplitude to be held fixed during measurement,
3. Measure the voltage across a load resistor ($R_L = Z_0$),
   (a) With no transmission line, measure V_0,
   (b) With a line of length, ℓ, inserted between the generator and R_L, measure $V\ell$,
4. Finally, calculate α_0 according to:

$$\alpha_0 = (1/\ell)\ 20 \log_{10} (V_0/V\ell) \qquad (3)$$

α_0 has the units db/m for ℓ measured in meters. To improve the accuracy of this measurement:

a. Make the generator impedance approximately Z_0,
b. Use a high impedance voltmeter,
c. Measure at several different lengths,
d. Repeat the measurement for several values of f_0, and, plotting log α_0 against log f_0, verify that your results are similar to **Fig. 8** (i.e., slope ≈ 0.5).

Now let's tackle propagation delay

Propagation delay imposed by a particular type of transmission line of length ℓ can be estimated using the α_0 vs. f_0 curve (such as **Fig. 8**) and the normalized time response curve of **Fig. 9.** The procedure is as follows:

1. Calculate α_0 for the length of cable to be used:

$$\alpha_0 = 6\text{dB}/\ell \text{ (in meters)} \qquad (4)$$

2. With α_0 from **Eq. 3,** enter **Fig. 8** (or a curve for the actual cable to be used) and read off a value of f_0, then compute t_0:

$$t_0 = 0.164/f_0 \qquad (5)$$

Here t_0 is in seconds when f_0 is in Hz.

3. You determine the propagation delay for a cable of the length selected in step 1 from the normalized curve in **Fig. 9.** This curve does not include source-to-load travel time; the time delay imposed by the cable response is measured from the time when energy begins to arrive at the termination. To find the delay for a HIGH-to-LOW transition t_{HL}, note the value of (t/t_0) in **Fig. 9** at which

$$e(t)/E = (V_{HIGH} - V_{thHL})/(V_{HIGH} - V_{LOW}) \qquad (6)$$

where V_{HIGH} and V_{LOW} are the asymptotic voltages and V_{thHL} is the HIGH-to-LOW threshold voltage.

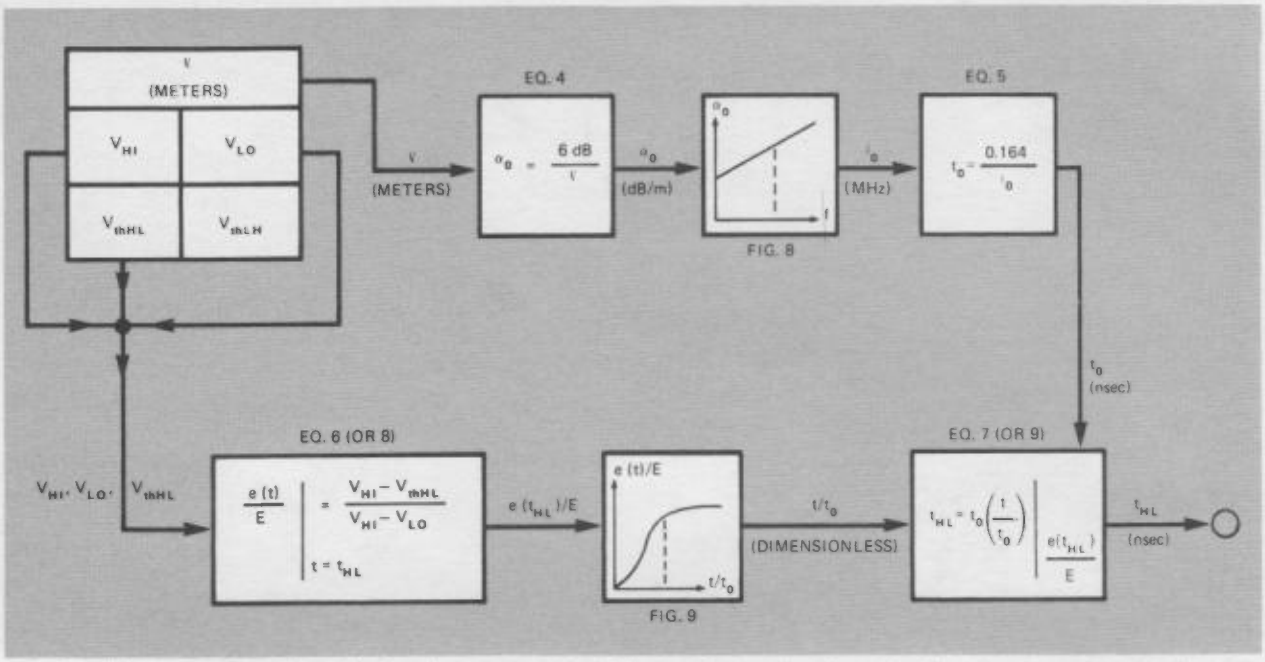
Then, with this value of (t/t_0), you can calculate the delay from

$$t_{HL} = t_0 \times (t/t_0) \qquad (7)$$

where t_0 is the value found in step 2, **Eq. 5.**

The delay for a LOW-to-HIGH transition is found similarly. From **Fig. 9** find (t/t_0) at which

$$e(t)/E = (V_{LOW} - V_{thLH})/(V_{LOW} - V_{HIGH}) \qquad (8)$$



Procedural flowgram summarizes the steps (see example) to follow in determining the cable delay time (t_{HL} or t_{LH}). Starting from known factors (ℓ, V_{HI}, V_{LO}, V_{thHL} and V_{thLH}), merely follow the flow and perform the calculations of each operator box. You can also work backwards: by knowing the steady state and threshold voltages and delay time, you can obtain cable length (ℓ).

Here V_{thLH} is the LOW-to-HIGH threshold. Then, with this value of (t/t_0), you again calculate the delay

$$t_{LH} = t_0 \times (t/t_0) \qquad (9)$$

An example makes it clear

Let's apply this procedure to a typical example that could crop up in a real-life situation. A μA9614 or DM8830 line driver with 75m of shielded twisted pair line with approximate load matching that has $V_{HIGH} = -2.14V$, $V_{LOW} = +2.14V$. (Inversion through the optoisolator accounts for the apparent polarity disparity.) For one side of the balanced pair, $V_{thHL} = V_{thLH} = 1.5V$.

1. From **Eq. 4,** calculate $\alpha_0 = 6dB/75m = 0.08$ dB/m
2. From **Fig. 8,** for $\alpha_0 = 0.08$ dB/m, read $f_0 = 14.2$ MHz. Then from **Eq. 5,** calculate $t_0 = 0.164/14.2$ MHz = 11.55 nsec
3. For t_{HL}, from **Eq. 6,** calculate:
   $e(t_{HL})/E = (-2.14 - 1.5)/(-2.14 - 2.14) = 0.85$
   Enter **Fig. 9** with $e(t)/E = 0.85$. Read off $(t/t_0) = 13$, and from **Eq. 7,** calculate:
   $t_{HL} = (11.55$ nsec $\times$ $(13) = 150$ nsec.

If we want to, we can work backwards. From given asymptotic (steady state) and threshold voltages, the value of e(t)/E is calculated from **Eq. 6** or **8,** and a value of t/t_0 is read from **Fig. 9.** Appiying the desired delay time to **Eq. 7** or **9** yields a value of t_0, and **Eq. 5** yields f_0. With this value of f_0, **Fig. 8** and **Eq. 4** can be used to determine either the maximum length of cable or the necessary cable characteristics for a desired length to achieve the desired delay.

Why not save some time?

Eqs. 4-9 and **Figs. 8** and **9** can also be used to examine effects of threshold and asymptotic voltage adjustments on delay times. While it is not likely that calculated results will agree precisely with measured performance, this procedure can save a great deal of design time by eliminating some possible causes of excessive propagation delay. Note, though, that you must remember that total propagation delay (t_{TPHL} or t_{TPLH}) includes that of the isolator itself (t_{PHL} or t_{PLH}). For example:

$$t_{TPHL}\text{ (total)} = t_{HL}\text{ (cable)} + t_{PHL}\text{ (isolator)} \qquad (10)$$

$$t_{TPLH}\text{ (total)} = t_{LH}\text{ (cable)} + t_{PLH}\text{ (isolator)} \qquad (11)$$

If the isolator delay times are relatively small, the importance of the cable-imposed delay time is emphasized. From **Fig. 9** and **Eqs. 6** and **8** it is clear that threshold voltages may profoundly influence the cable-imposed delay. Ideally, the HL and the LH thresholds should be balanced, so **Eqs. 6** and **8** yield equal values of e(t)/E, resulting in balanced delays. The use of hysteresis in the termination tends to give larger values in both **Eqs. 6** and **8,** whether balanced or not, while the use of peaking in the termination tends to reduce both. Thus, while hysteresis is helpful in prevent-

ing errors due to noise (either common mode or differential mode), its adverse effect on data rate should be considered.

Interference protection. A final, but important, cable consideration is its property of common-mode rejection (CMR). The cable cannot relieve the effects of common-mode signals generated within the equipment being interconnected, but it can reduce the effects of induced interference. Either inductively or capacitively induced common-mode signals are less likely to occur in balanced lines than those that are single ended. If we rank lines in descending order of CMR effectiveness, we rate shielded twisted pair first, then unshielded twisted pair and finally coaxial.

If your system requires a data rate capability that only coaxial line can provide, but if the coaxial line does not give adequate CMR, then a pair of coaxial lines should be used for each channel. By driving the two coaxial lines in opposite phase, a balanced system is obtained, having the data rate capability of coaxial line and a CMR at least as good as shielded twisted pair. We will reserve a more detailed discussion of CMR enhancement for a later article. □

References

1. "Performance of the 5082-4350/51/60 Series of Isolators," Application Note AN-948, Hewlett-Packard.
2. Dreher, Thad, "Cabling fast pulses? Don't trip on the steps," The Electronic Engineer, Aug. 1969, pp. 11–75.

Part 2 of this series will examine resistive terminations to achieve on/off steady-state conditions, optimize data rate and reduce reflections in short, low-loss lines.

Author's biography

Hans Sorensen is an applications engineer at the HPA Div. of Hewlett-Packard in Palo Alto, CA. His duties include appnote preparation and technical-applications assistance concerning optoelectronic devices. He received his BSEE from Illinois Institute of Technology and his MSEE from Stanford Univ. Mr. Sorensen holds one patent on an optical-beam position detector, and he is a member of IEEE.

Designer's Guide to: Optoisolators—Part 2

If you're looking for simplicity and economy in your line terminations, the resistive road is the one to take.

Hans Sorensen, Hewlett-Packard, HPA Div.

Ignore proper termination of a high-speed digital transmission line and you'll pay several times over: either the line receiver won't switch or line reflections will play a game of Russian Roulette with the receiver, producing multiple switching. Or your high-speed printer will crawl at half speed. Or any of a dozen other unpleasant surprises will await you.

With an optoisolator as the active element in a line receiver, designing a resistive termination becomes more complicated than merely connecting a terminating resistor across the line. This is because you must account for forward voltage (V_F) and forward current (I_F) requirements of the optoisolator input diode. There's little current flow until the diode voltage exceeds V_F. Then V_F remains substantially constant as current increases. Input current must be high enough for proper operation of the photodetector and output circuit, but it must not exceed maximum ratings.

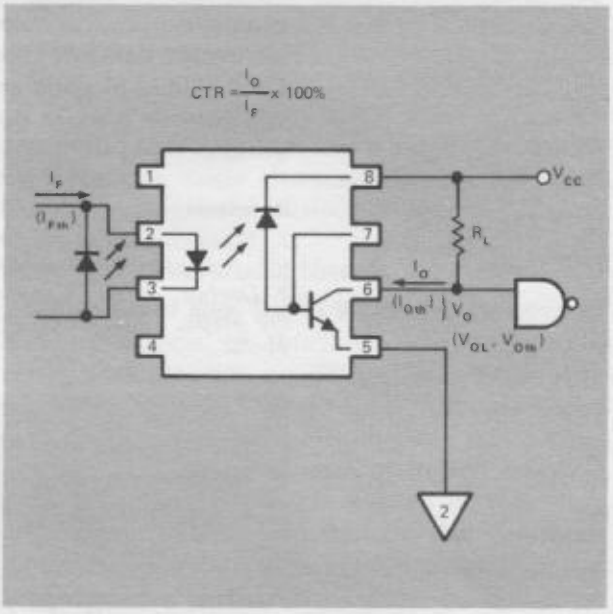


Fig. 1—Proper steady-state current drive (I_F) is determined by the maximum I_O needed to drive the output logic, as well as V_{CC}, V_{OL}, and current transfer ratio (CTR). Designing for extra drive (up to 20%) will compensate for CTR degradation.

Three Commandments of termination design

Three design objectives must be considered when terminating any line:

1. Proper ON/OFF steady-state conditions (I_F);
2. Threshold adjustment (I_{Fth}) for optimum data rate (unequal thresholds will time-distort data pulses);
3. Load matching to reduce reflections in low-loss, high-speed lines less than 50 meters long.

The first design objective is mandatory! You must always meet it or the optoisolator will simply not provide sufficient drive for the logic—possibly even none at all. Objectives 2 and 3 are desirable but not always mandatory; in some cases they may be impossible. For example, you can't balance thresholds with a single isolator if polarity-reversing drive is used.

Generally, while a 3-resistor termination meets all three objectives, a 1-resistor meets only one (1), and a 2-resistor termination meets two (1 and 2 or 1 and 3).

Proper min./max. current limits must be observed to ensure reliable optoisolator switching. The minimum current for some types of isolators is established by the manufacturer. For others, it depends on the isolator's current transfer ratio (CTR) and the output logic drive requirements.

When selecting input current (I_F), you should allow

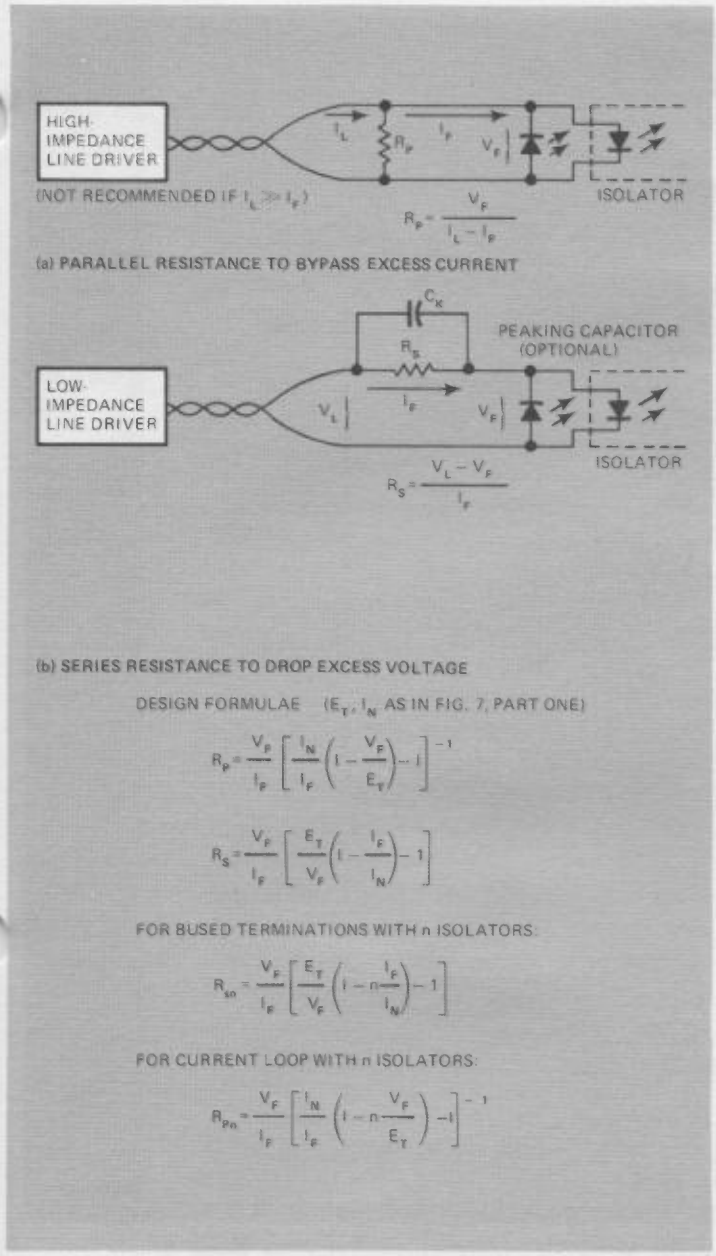


Fig. 2—One-resistor terminations will meet design Objective 1 (steady state). Parallel-resistance circuit **(a)** possesses poor regulation, but responds more rapidly. Series-resistance termination **(b)** handles a wider range of source voltages but is inherently slower. Its response time can be improved by shunting the series resistor with a peaking capacitor (C_K), provided an anti-parallel LED is placed across the optoisolator input to discharge C_K. Otherwise, the anti-parallel LED is employed only with polarity-reversing drive.

for CTR degradation. CTR decreases rapidly at high levels of input current. Typically, at $I_F > 20$ mA, allow an extra 20%. But at $I_F < 2$ mA, a 5% margin is adequate for more than 20,000 hrs. of proper operation.

To design a termination, begin with the heart of the receiving module—the optoisolator—and find a nominal value for the minimum input current (**Fig. 1**). For the steady ON state, the voltage drop across R_L must be large enough to make V_O adequately low with respect to the logic family used at the output.

Calculate the maximum value of I_O, taking account of the tolerance on R_L and maximum V_{CC}. Then divide by the minimum CTR to arrive at the proper value of I_F. However, since the manufacturer sometimes specifies a minimum CTR for only one value of I_F, you might want to try an alternate (and preferred) procedure. Use the known value of I_F and the minimum CTR to find the minimum value of R_L:

$$I_F \geq I_O\ (\text{max.}) \times \left[\frac{100\%}{\text{CTR (min.)}}\right] =$$

$$\left[\frac{V_{CC}\ (\text{max.}) - V_{OL}\ (\text{min.})}{R_L\ (\text{min.})}\right] \times \left[\frac{100\%}{\text{CTR (min.)}}\right] \quad (1)$$

For the steady OFF state, reduce the input current to a value at which the output is at a proper logic HIGH level.

Protect the input diode from excessive reverse current when using polarity-reversing drive. The best way is to shunt the input diode with a LED having the same forward voltage as the isolator input diode, but with opposite polarity (**Fig. 1**).

One-resistor termination—the economy line

If the transmission line is long, has a high resistance and carries a low data rate, then Objective 1 is your only worry. Therefore, the 1-resistor termination is your choice, and design of the termination will be as simple as in **Fig. 2,** leaving you nothing further than a decision between the two versions.

Parallel-resistance termination (Fig. 2a) permits the input photodiode to face a lower source resistance and, thereby, to respond more rapidly. But since the circuit trades speed for poorer regulation, it should be avoided unless the open-circuit voltage, E_T, is several hundred mV greater than V_F. Also, the line current I_L must not be more than twice the value of I_F.

Series-resistance termination (Fig. 2b) can handle a broader tolerance on the resistance value and source characteristics. Although the high source resistance imposed on the input diode tends to reduce the speed of response, connecting a peaking capacitor (C_K) in parallel with R_S can compensate for this effect.

Both series- and parallel- resistance terminations in reverse-polarity should have an anti-parallel diode across the input of the opto-isolator, since reverse current may reduce the CTR by heating the input diode. If you use a peaking capacitor in the series termination, always use the anti-parallel LED — whether the drive is reversing or not. This gives the peaking capacitor a chance to discharge for maximum peaking.

When multiple terminations are on one line

Can several optoisolators operate on the same

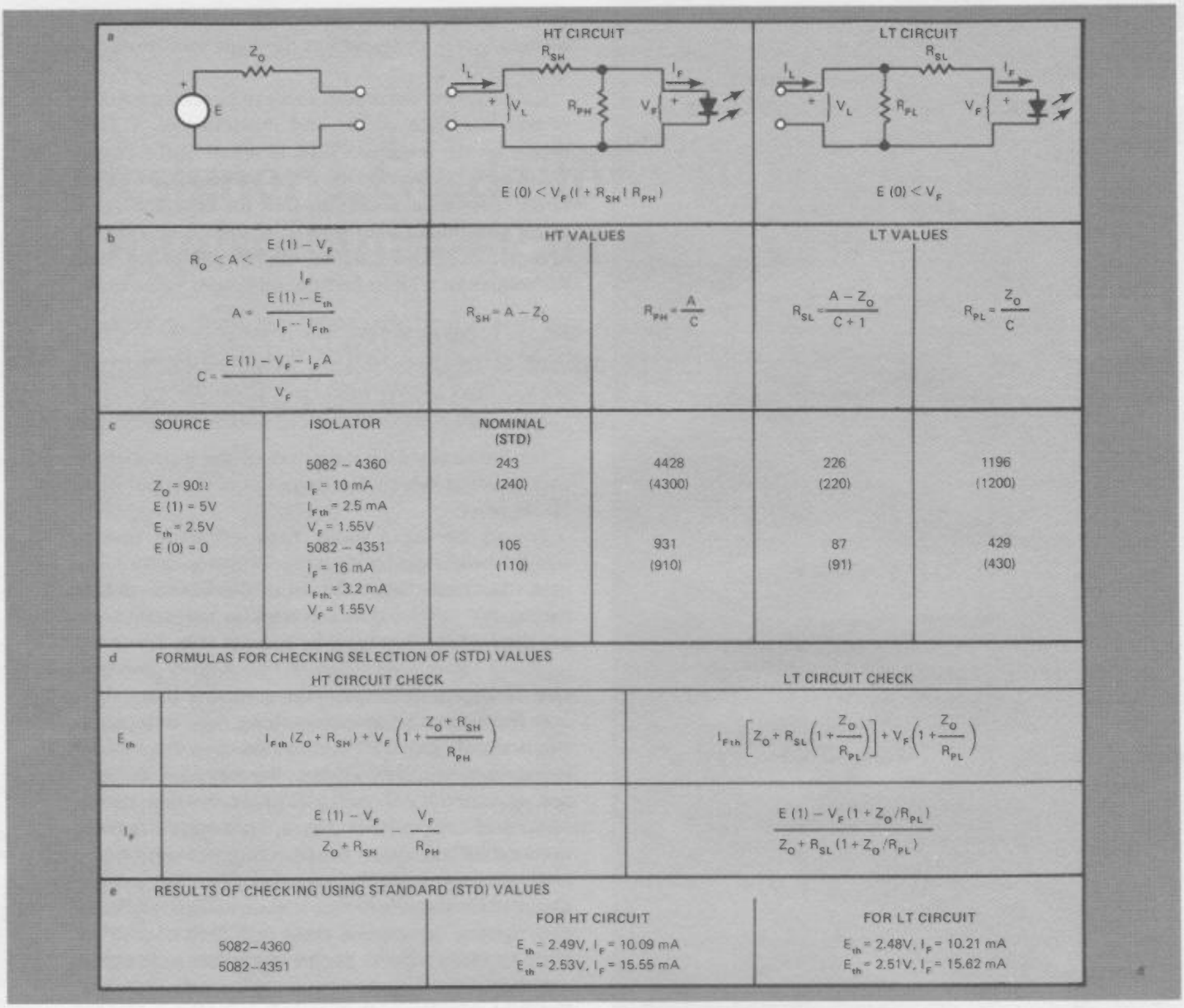


Fig. 3—Two-resistor termination circuits (a) for a back-matched ($R_g = Z_0$), polarity nonreversing system. Obtain the line impedance, optoisolator data and steady-state threshold values. Calculate 'A' and 'C', making sure that 'A' falls within the calculated limits **(b)**. Then calculate the series and parallel resistance **(b)** and choose the closest standard values as illustrated in the two examples **(c)**. To be sure threshold and steady-state conditions are still met by the standard values, calculate E_{th} and I_F **(d)** as demonstrated in the two examples **(e)**.

transmission line? Yes, but be sure to use the series-resistance termination with a separate resistance (and, if required, an anti-parallel LED) for each isolator input. To find the value of resistance to be used for bused terminations, refer to the formula for R_{Sn} in **Fig. 2.** Obviously, if $I_F \ll I_X$, the value of R_{Sn} will not change much as n, the number of terminations, varies. Under these conditions, terminations can be added or removed without disturbing existing ones.

The parallel-resistance termination is not suitable for busing. However, it could be used in a current loop, with several isolator inputs connected in series and a separate R_{Pn} across each.

What's threshold adjustment?

Between the steady-state extremes for logic ZERO and logic ONE, a voltage level exists at which transition occurs. The amplitude of this threshold level, relative to the asymptotic levels (upper and lower extremes), can seriously affect propagation delay. To correct this, raise the threshold to lengthen HL (High-Low) delay and shorten LH delay or vice versa. Remember, for optimum error-free data rate, the overall delays should balance; or, in a word, $t_{TPHL} = t_{TPLH}$.

In cases where cable-imposed delays greatly exceed isolator delays, threshold adjustment can work wonders. Where cable delays are negligible relative

to isolator delays, though, threshold adjustment will still influence HL and LH delays as described above, although the amount of influence can't be calculated.

To find the threshold level for the output circuit **(Fig. 1),** I_{Fth} is substituted into **Eq. 1** to yield:

$$I_{Fth} = I_{Oth}\ (typ.) \times \left(\frac{100\%}{CTR\ (typ.)}\right) =$$

$$\left[\frac{V_{CC}\ (typ.) - V_{Oth}\ (typ.)}{R_L\ (typ.)}\right] \times \left[\frac{100\%}{CTR\ (typ.)}\right] \quad (2)$$

Since the values called for are typical rather than maximum or minimum, it may be necessary to obtain them empirically.

Are two resistors better than one?

If you find your data rate is high enough to be time-distorted by unequal leading- and trailing-edge thresholds, you have an unbalanced system. Except for isolated cases, the old 1-resistor trick won't work here.

First, find I_F and I_{Fth} from **Eqs. 1** and **2.** Then decide how to arrange the two resistors **(Fig. 3),** either in the High Threshold (HT) or Low Threshold (LT) termination. Incidentally, the HT and LT designations refer to the voltage threshold at which the isolator input diode begins to conduct significantly.

In making your choice, remember that for significant diode conduction (hence, impedance lowering), the LT circuit requires only that $V_L > V_F$; while the lower impedance HT circuit requires that $V_L > V_F\ (1 + R_{SH}/R_{PH})$.

The design relationships of **Fig. 3** hold for a back-matching system ($R_g = Z_0$) with negligible wire resistance. E(1) is the open-circuit voltage for isolator-ON state, and E(0) is the open-circuit voltage for the isolator-OFF state. To place the threshold voltage at any desired midway value, use a resistor network at the driver to raise E(0) to the required voltage, such that:

$$E_{th} = \frac{[E(1) + E(0)]}{2} \quad (3)$$

The only limitation on E(0) is that V_L be less than the impedance threshold value, which requires $E(0) < V_F$ for the LT circuit, and $E(0) < V_F\ (1 + R_{SH}/R_{PH})$ for the HT.

For designing the HT circuit, follow the design expressions in **Fig. 3.** If you care to verify the expressions, solve for R_{SH} and R_{PH} in the pair of simultaneous equations resulting when E_{th} and I_{Fth} are substituted for E(1) and I_F in the HT circuit equation:

$$\frac{E(1) - V_F}{Z_0 + R_{SH}} - \frac{V_F}{R_{PH}} = I_F \quad (4)$$

The design expressions for the LT circuit are found by solving for R_{PL} and R_{SL} in the pair of simultaneous equations obtained by substituting E_{th} and I_{Fth} for E(1) and I_F in the LT circuit equation:

$$\frac{(E(1) - I_F Z_0)}{\left(\frac{1 + Z_0}{R_{PL}}\right)} - I_F\, R_{SL} = V_F \quad (5)$$

As a matter of interest, notice that as the value of "A" **(Fig. 3)** approaches either of its limits, the HT and LT circuits become identical, reducing to either a series or parallel 1-resistor termination. On the other hand, if "A" falls outside the prescribed limits, the first method fails and a solution for the selected value of E_{th} does not exist.

To remedy this situation, substitute E_{th} from **Eq. 3** into the expression for "A" and its limits **(Fig. 3).** This yields:

$$Z_0 < \frac{(E(1) - E(0))}{2(I_F - I_{Fth})} < \frac{(E(1) - V_F)}{I_F} \quad (6)$$

When the system is not back matched or when the wire resistance is significant, a specific solution for either the HT or the LT circuit becomes too complicated. Instead, use the following alternate approximation procedure that converges onto the solution.

Obtain E_T for both the ONE and ZERO state and use them as E(1) and E(0), respectively. Terminate the line with a variable resistor and plot line current as a function of line voltage **(Fig. 7** of **Part 1).** Next, project the linear portion of the curve to both axes and read I_N and E_T. For Z_0 use $R_{DC} = E_T/I_N$. Then apply the equations in **Fig. 3** to compute resistor values. Try the circuit, don't be surprised if it doesn't work. Recompute, if necessary, selecting a different value of E_{th}. Keep at it until you obtain values that produce a balanced delay.

Reflecting on the problem

In high-speed data transmission lines under 50 meters, reflections can kill your system. Reflection occurs when a transient propagating along a transmission line encounters an impedance not equal to the line's characteristic impedance. And just as echoes can make conversation unintelligible in a canyon, so too, can these electrical reflections transform data flow into gibberish. If this is your problem, consider these two alternatives.

One method uses "load matching" to make the termination impedance match the line, so all incident energy is absorbed. Presto, no reflection! On the other hand, "back matching" matches the drive (generator) impedance to the line. One reflection may occur, but is absorbed at the driver.

For linear impedances, the magnitude and polarity of reflections can be computed from the reflection coefficients ρ_ℓ and ρ_g:

$$\rho_\ell = \frac{(R_\ell - Z_0)}{(R_\ell + Z_0)} \qquad \rho_g = \frac{(R_g - Z_0)}{(R_g + Z_0)} \quad (7)$$

$$(\Delta \overleftarrow{V}_L) = \rho_\ell\, (\Delta \overrightarrow{V}_L) \qquad (\Delta \overrightarrow{V}_L) = \rho_g\, (\Delta \overleftarrow{V}_L) \quad (8)$$

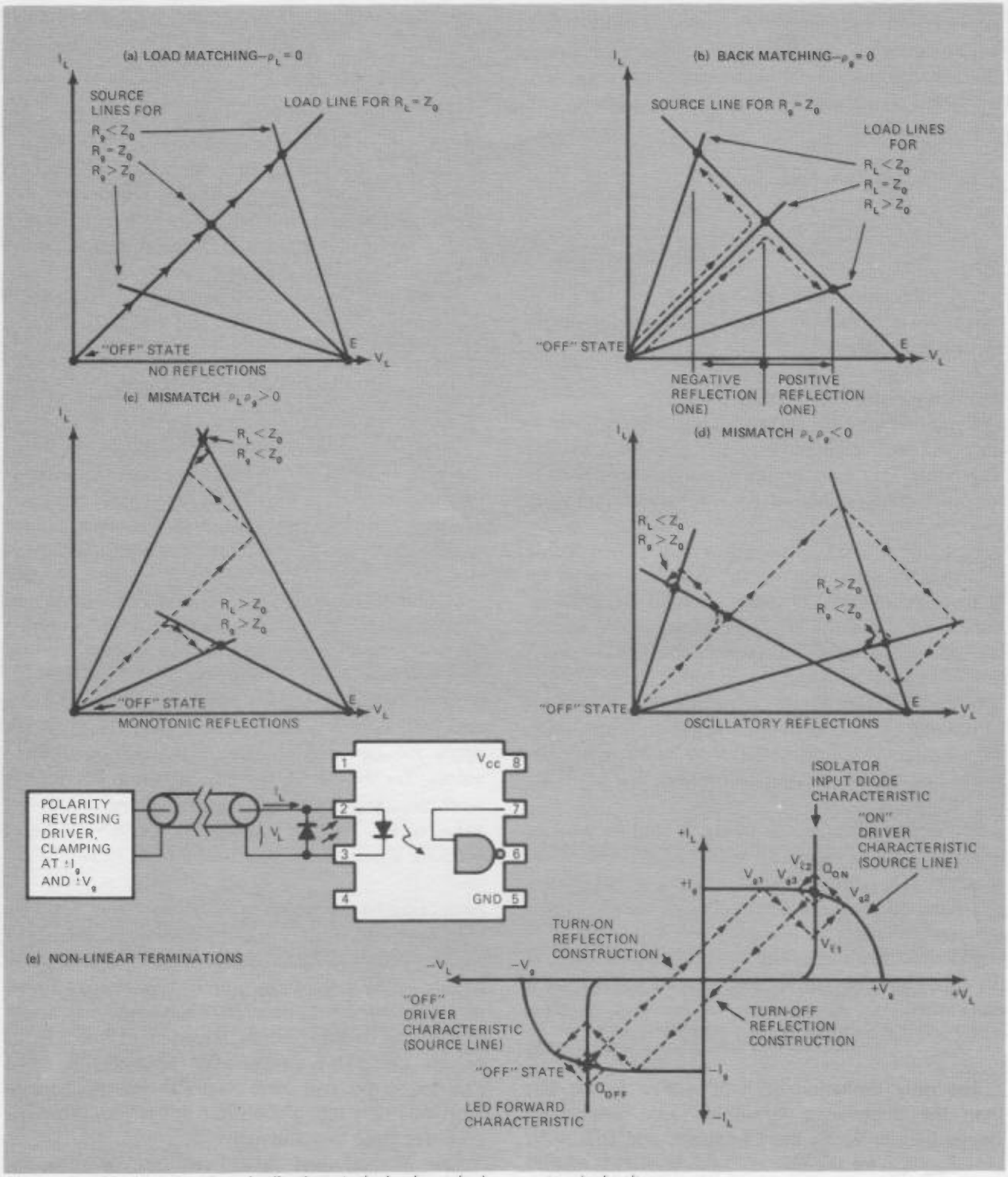


Fig. 4—Graphical construction of reflections. In the load-matched ($R_L = Z_0$) system, the termination absorbs all incident energy **(a)**. With a back-matched ($R_g = Z_0$) system, incident energy reflected back from the termination is absorbed by the driver **(b)**. A double-mismatch of both driver and receiver to the line, but with like polarity, leads to monotonic reflections **(c)** that limit data rate. But double-mismatched systems with opposite polarity produce oscillatory re-reflections **(d)** that cause multiple switching. In **(d)**, both turn-on and turn-off reflections are plotted for a nonlinear system.

Step-by-step example:

To examine reflections as a change is made from the OFF state to the ON state, let's plot them for a nonlinear system **(Fig. 4e)**:

1. Beginning at the OFF-state quiescent point (Q_{OFF}), draw a line with a positive slope, $(\Delta V_L/\Delta I_L) = Z_0$, to the point where it intersects the "source line." This gives the initial generator terminal voltage, v_{g1};
2. From v_{g1} on the "source line," draw a line with negative slope, $(\Delta V_L/\Delta I_L) = -Z_0$, to where it intersects the "load line." This gives the initial load terminal voltage, $V_{\ell 1}$;
3. From $V_{\ell 1}$ on the "load line," draw a line with positive Z_0 slope to v_{g2} on the "source line";
4. From v_{g2} on the "source line," go along a negative Z_0 slope to $v_{\ell 2}$ on the "load line";
5. From $v_{\ell 2}$ on the "load line," go along a positive Z_0 slope to v_{g3} on the "source line";
6. Repeat this procedure until the construction converges at the ON-state quiescent point (Q_{ON}). A positive Z_0 slope is used in moving toward a point on the "source line" and a negative Z_0 slope is used in moving toward a point on the "load line."

To plot the turn-OFF reflections, begin at the Q_{ON} point and follow the above procedure.

($\Delta\vec{V}_L$) is a transient propagating toward the load and ($\Delta\overleftarrow{V}_L$) is a transient propagating toward the generator. R_ℓ is at the load and R_g is at the driver.

Incidentally, the above reflection coefficients apply only to the line voltage step change, ΔV_L.

Have nonlinearities got you down? If so, you will find it more practical to use a graphical construction to examine reflections. This technique can handle nonlinear impedances because it takes account of the instantaneous line voltage (and current) as well as of the step change. Construct the graph (**Fig. 4**) on linear coordinates of line current (I_L) and line voltage (V_L). First, draw the "load line"—the V-I characteristic of the load (positive current flows into the LOAD). Next, construct the "source lines"—one for logic ONE (ON) state and another for logic ZERO (OFF) state. These are the V-I characteristics of the source (positive current flows from the source into the line). Finally, graph the reflections.

Incidentally, we show the driver characteristics represented in **Fig. 4e** only for illustration. Yes, the circuit can be used, but it would prove a disaster in any high-speed system.

Various combinations of load/source match/mismatch for polarity nonreversing drive provide better solutions to the problem. In order of desirability, they are:

- BEST—**Fig. 4a**—load matching allows no reflections regardless of source mismatch polarity or magnitude.
- NEXT BEST—**Fig. 4b**—back matching allows one reflection regardless of load mismatch polarity or magnitude.
- TOLERABLE—**Fig. 4c**—double mismatch, same polarity, $\rho_\ell \rho_g > 0$—may have several re-reflections, but both source and load terminal voltages approach steady-state condition monotonically, so the only effect is a data rate limitation depending on magnitude of $\rho_\ell \rho_g$.
- POTENTIALLY DISASTROUS—**Fig. 4d**—double mismatch opposite polarity, $\rho_\ell \rho_g < 0$—oscillatory re-reflections; not only is data rate limited, but there is high risk that a single HL or LH transition may produce multiple transitions (HL − LH − HL) in the output circuit, especially with a short (< 50m) line. □

This Designer's Guide series has now expanded to five parts. The third part will continue the discussion of resistive terminations, focusing on load matching with 2-resistor terminations and applications for 3-resistor terminating networks.

Designer's Guide to: Optoisolators—Part 3

These design procedures permit 2- and 3-resistor terminations to adjust threshold, match impedances and boost system performance.

Hans Sorensen, Hewlett-Packard, HPA Div.

Last issue we covered 1- and 2-resistor termination designs; this article delves into 3-resistor designs and the use of 2-resistor circuits in impedance-matching. As we saw, there are three design objectives in termination design: forward isolator drive (I_F), threshold balancing and impedance matching. One-resistor terminations meet only the first goal; two resistors meet two goals; while three resistors meet all three goals.

Matching loads? Two resistors will do!

Under certain conditions, a 1-resistor termination can simultaneously satisfy Objective 1 and Objective 3 (load matching):

- If $R_g < Z_0$ and $R_P < Z_0$, **(Fig. 2a, Part 2)**
- If $R_g > Z_0$ and $R_S > Z_0$, **(Fig. 2b, Part 2)**

In general, however, two resistors are required to satisfy the two objectives (1 and 3, Part 2). As we already know, **Eq. 1** simply establishes the proper value

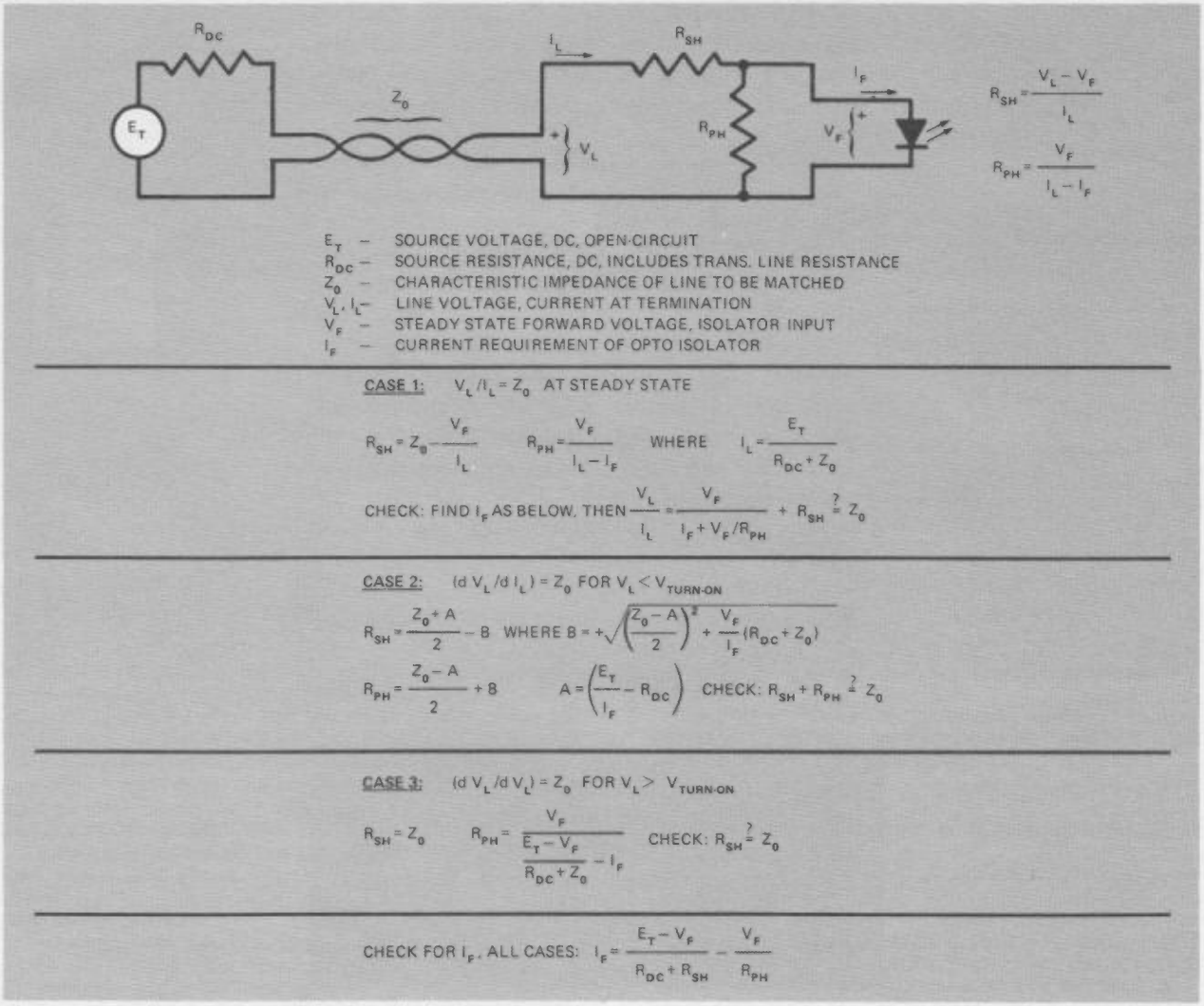


Fig. 1—Approximate load matching for HT circuits. Dynamic resistance of the terminating circuit ($\partial V_L/\partial I_L$) changes as the optoisolator switches ON. These three cases are calculated differently as shown.

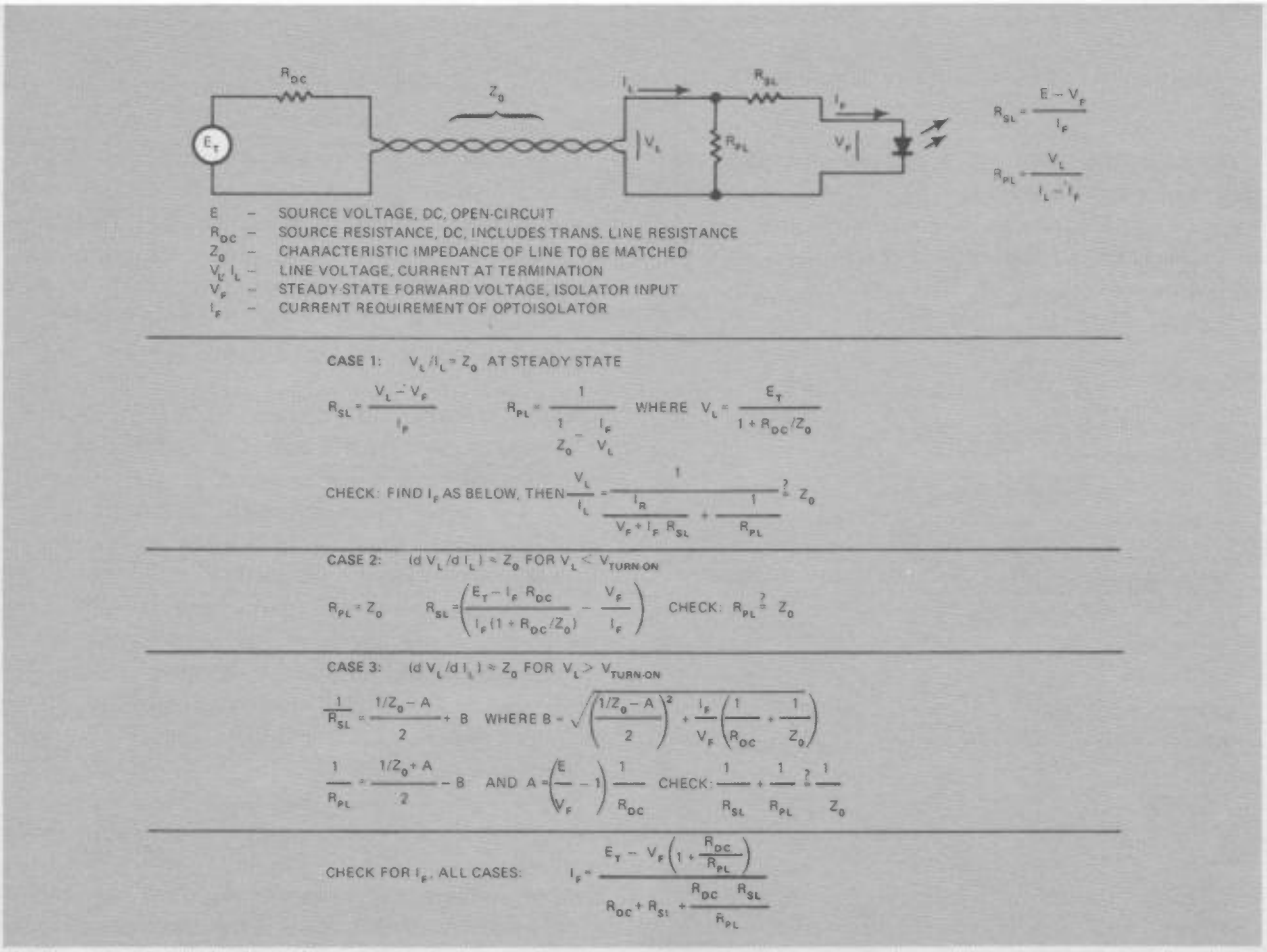


Fig. 2—Approximate load-matching LT circuit design formulas. After calculating series and parallel resistances, select the closest standard values and check I_F with these values to determine if the practical circuit is satisfactory.

for I_F. The dynamic resistance of the termination changes as the isolator input diode goes from OFF to ON. To satisfy Objective 3 (approximate load matching), we must consider three cases produced by this change of dynamic resistance of the termination:

CASE 1: $V_L/I_L = Z_0$. The reflection coefficient, which is the ratio of voltage in the reflected wave to the incident wave, changes from positive to negative as the input diode turns ON. This is the best choice for a back-matched driver or one of unknown reflection coefficient; and though it may permit oscillatory reflections, they will be of low amplitude. That's not bad, considering it's the easiest termination to design.

CASE 2: $\partial V_L / \partial I_L \leq Z_0$. The reflection coefficient changes from zero to negative as the input diode turns ON. This permits a larger reflection than CASE 1, but prevents oscillatory reflection for a driver with $R_g < Z_0$.

CASE 3: $\partial V_L / \partial I_L \geq Z_0$. Reflection coefficient changes from positive to zero as the input diode turns ON. This permits a larger reflection than CASE 1, but prevents oscillatory reflection for a driver with $R_g > Z_0$.

An HT or an LT circuit can satisfy these three conditions. The expressions for selecting R_{SH} and R_{PH} for the HT circuit are given in **Fig. 1;** the expressions for R_{PL} and R_{SL} for the LT circuit, in **Fig. 2.**

For CASE 1, the design expressions that result from the circuit equations are as follows.

For the HT circuit:

$$R_{SH} = \frac{(V_L - V_F)}{I_L} \qquad R_{PH} = \frac{V_F}{(I_L - I_F)} \tag{1}$$

For the LT circuit:

$$R_{SL} = \frac{(V_L - V_F)}{I_F} \qquad R_{PL} = \frac{V_L}{(I_L - I_F)} \tag{2}$$

V_L and I_L have the values resulting when a resistor whose value is Z_0 is connected to the source (including cable) whose characteristics are determined as in **Fig. 7** of **Part 1:**

$$V_L = E_T\left(1 + \frac{E_T}{I_N Z_0}\right)^{-1} \qquad I_L = \left(\frac{E_T}{Z_0}\right)\left(1 + \frac{E_T}{I_N Z_0}\right)^{-1} \tag{3}$$

E_T and I_N are measured for the logic state that turns the isolator input diode ON, so $E_T = E(1)$; the assumption is that E(0) is low enough to produce turnoff.

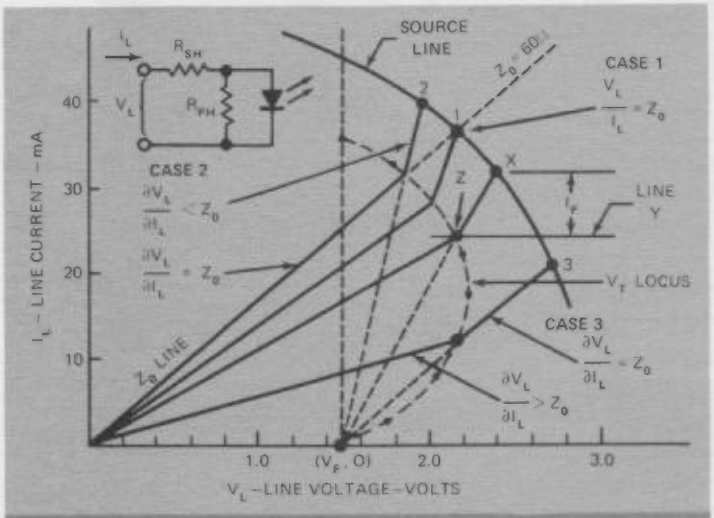
For CASE 2 and CASE 3, the design expressions

result from the assumption that the dynamic resistance of the isolator input diode is infinite below turn-on and a short-circuit above turn-on. Applying this condition to the circuit equations yields the following relations:

For the HT circuit:

$$\frac{E_T - V_F}{\left(\frac{E_T}{I_N} + R_{SH}\right)} - \frac{V_F}{R_{PH}} = I_F$$

CASE 2: $R_{SH} + R_{PH} = Z_0$ **(4)**



GENERAL CONSTRUCTION FOR ANY POINT, X ON THE SOURCE LINE:

1. DRAW CONSTANT-CURRENT LINE Y AT I_F BELOW X
2. DRAW LINE FROM X TO $(V_F, 0)$, INTERSECTING Y AT Z
3. LINE OZ HAS SLOPE $\frac{\partial I_L}{\partial V_L} = \frac{1}{R_{SH} + R_{PH}}$; ZX HAS SLOPE $\frac{\partial I_L}{\partial V_L} = \frac{1}{R_{SH}}$

CASE 1: DRAW Z_0 LINE TO INTERSECT SOURCE LINE AT $\frac{V_L}{I_L} = Z_0$ THEN PROCEED AS FOR POINT X

CASE 2: CONSTRUCT LOCUS OF TURN-ON VOLTAGES (Z POINTS). WHERE LOCUS INTERSECTS Z_0 LINE IS TURN-ON VOLTAGE FOR CASE 2. FROM THIS POINT DRAW LINE THROUGH $(V_F, 0)$ TO INTERSECT SOURCE LINE AT "2"

CASE 3: FROM $(V_F, 0)$ DRAW LINE WITH SLOPE $1/Z_0$ TO POINT 3 THEN PROCEED AS FOR POINT X

Fig. 3—Graphical construction procedure for an HT circuit with a nonlinear source.

CASE 3: $R_{SH} = Z_0$

For the LT circuit:

$$\frac{(I_N - I_F)}{\left(\frac{I_N}{E_T} + \frac{1}{R_{PL}}\right)} - (I_F R_{SL}) = V_F$$

Case 2: $R_{PL} = Z_0$ **(5)**

CASE 3: $\frac{1}{R_{PL}} + \frac{1}{R_{SL}} = \frac{1}{Z_0}$

E_T and I_N are described earlier for **Eq. 3. Figs. 1** and **2** summarize HT and LT circuit design formulas, approximate matching and steady-state requirements.

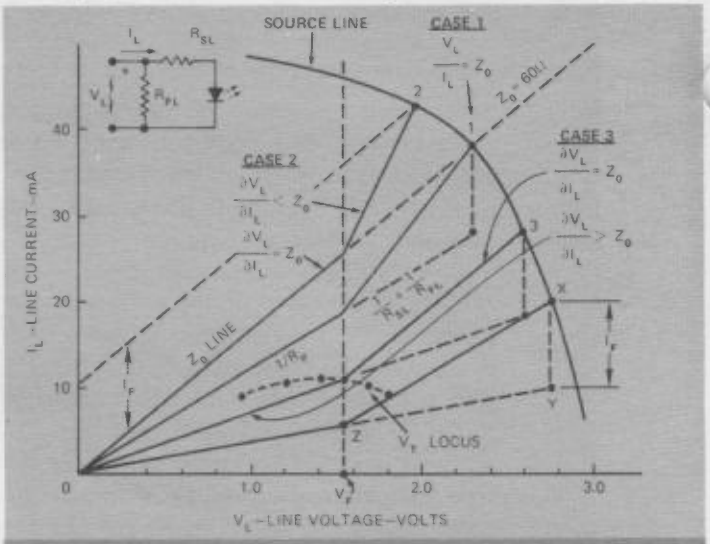
Graphical solutions for load matching are the only practical, handy tools available to design with nonlinear sources. Even with linear sources, there's an advantage to working with graphical solutions—they literally make the design tradeoffs clearly visible! (For further design of load-match terminations, refer to **Fig. 3** of **Part 2** and **Fig. 3** of this article).

Consider the HT vs. LT circuit

So you've decided the 2-resistor termination is for your line receiver, have you? Well, you still must make one more decision: High Threshold vs. the Low Threshold circuit. Consider the advantages of both before making your choice.

In general, HT and LT circuits have the same relative merits, respectively, as the parallel and series 1-resistor terminations, and for the same reason. The HT circuit is faster, but more vulnerable to driver variations and resistor tolerances. Thus it's not suitable for busing.

If you want to go the bus route, be advised that busing with the LT circuit is possible within the limits of available current from the driver. When busing n isolators, obtain the values of R_{PL} and R_{SL}. How? Simply substitute $n \times I_F$ for I_F in the formulas of **Fig. 2,** or the graphical construction of **Fig. 4.** Then, in series



GENERAL CONSTRUCTION FOR ANY POINT, X, ON SOURCE LINE:

1. FROM POINT Y AT A CURRENT I_F BELOW X, DRAW LINE TO ORIGIN, INTERSECTING V_F LINE AT Z
2. LINE OZ HAS SLOPE $\frac{\partial I_L}{\partial V_L} = \frac{1}{R_{PL}}$
3. LINE ZX HAS SLOPE OF $\frac{\partial I_L}{\partial V_L} = \frac{1}{R_{PL}} + \frac{1}{R_{SL}}$

CASE 1: DRAW Z_0 LINE TO INTERSECT SOURCE LINE AT $\frac{V_L}{I_L} = Z_0$ THEN PROCEED AS FOR POINT X

CASE 2: DRAW LINE PARALLEL TO Z_0 THROUGH A POINT I_F ABOVE THE Z_0 LINE TO WHERE IT INTERSECTS THE SOURCE LINE AT 2; THEN PROCEED AS FOR X

CASE 3: CONSTRUCT V_T' LOCUS BY DRAWING LINES WITH SLOPES $1/Z_0$ FROM POINTS X' ON SOURCE LINE, INTERSECTED BY LINES FROM O TO POINTS AT I_F BELOW EACH X'. EACH INTERSECTION, Z' IS A POINT ON THE V_T' LOCUS. WHERE THE V_T' LOCUS INTERSECTS THE V_F LINE IS THE Z POINT FOR CASE 3. A LINE FROM HERE TO THE SOURCE LINE WILL HAVE A SLOPE, $1/Z_0$

Fig. 4—Graphical construction procedure for a LT circuit with a nonlinear source.

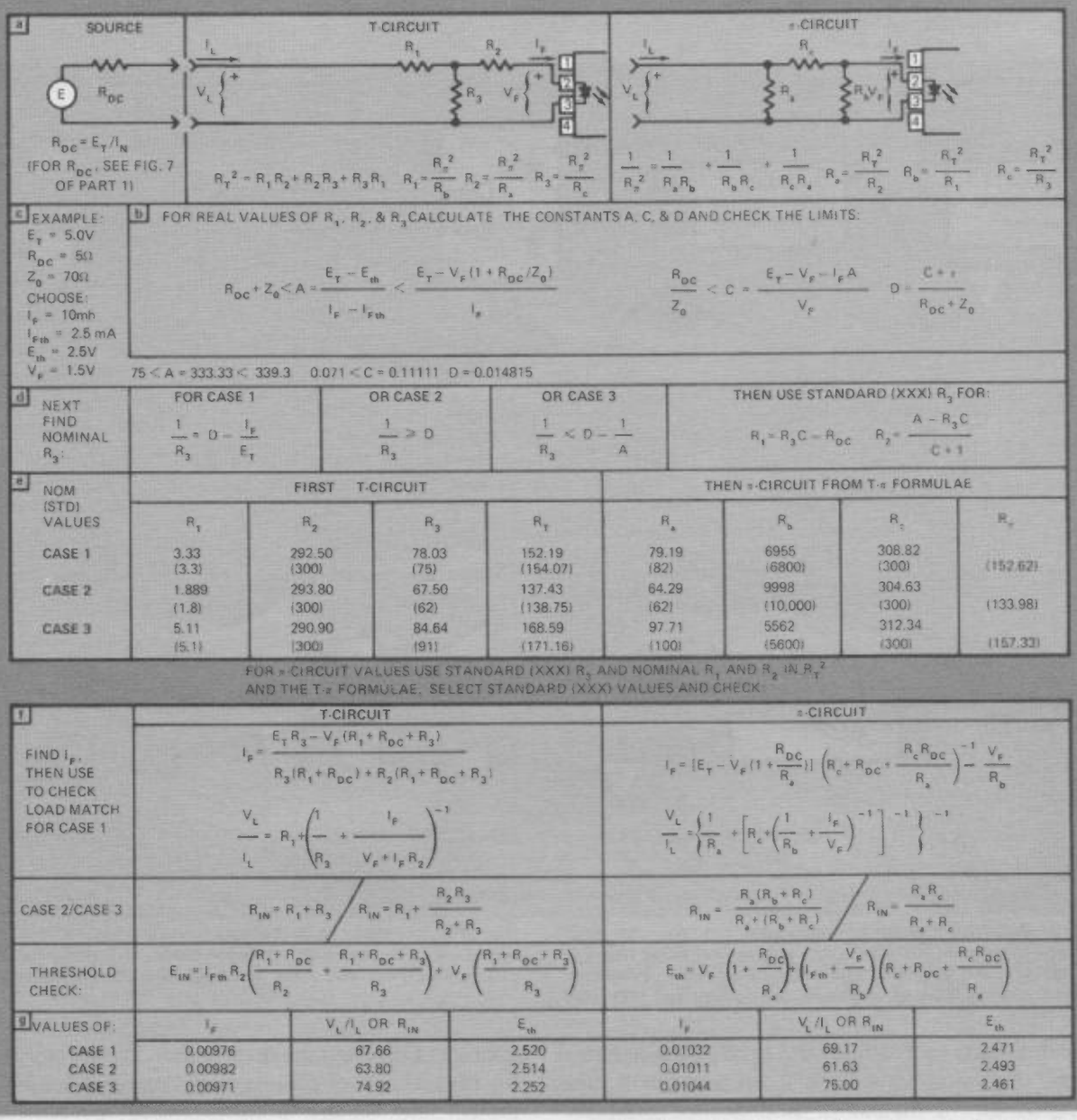


Fig. 5—This 3-resistor termination design procedure calculates the T-circuit first, then converts to π-values **(a)** and determines which set of nominal values are closest to standard resistors. First, calculate 'A', 'C' and 'D' and be sure they fall within the limits **(b)** as demonstrated by the example **(c)**. Second, calculate R_3 and then solve for both R_1, R_2 **(d)** and R_T, as in the example **(e)**. Fourth, convert to the π-circuit. Finally, select standard resistor values and check I_F, V_L/I_L and E_{th} for the three cases **(f)** as in the example **(g)**.

with each isolator input use n × R_{SL}, where R_{SL} is the value obtained by making the n × I_F substitution. Finally, connect a single R_{PL} (serving the n isolators) across the line.

If you're lucky, the current (I_F) required by the isolator will be such a small fraction of the current available that busing can be done without making any resistor value adjustment. If so, fine.

For current-loop designs, neither the HT nor the LT circuit is very good and the parallel 1-resistor circuit described earlier must be used. If this won't meet the objectives of your line and receiver, then consider using active or 3-resistor terminations.

Believe me, three is best

As we saw earlier, 2-resistor terminations can handle Objectives 1 and 2 or Objectives 1 and 3. Yes, in special situations (wonder of wonders!) it just *might* happen that a 2-resistor termination could meet all three objectives—but don't count on it. As a rule of thumb, it takes a 3-resistor termination to meet all three objectives.

Fig. 5 shows the circuit to be used and expressions for computing the nominal resistor values. The basic expressions are given only for the T-circuit because those for the π-circuit are unwieldy. Since the T and π-circuits are electrically identical, the T-π transformation can be used to obtain nominal π-circuit resistance values that may be closer to standard ones than the nominal values computed for the T circuit. Then the π-T transformation can be used to check the design.

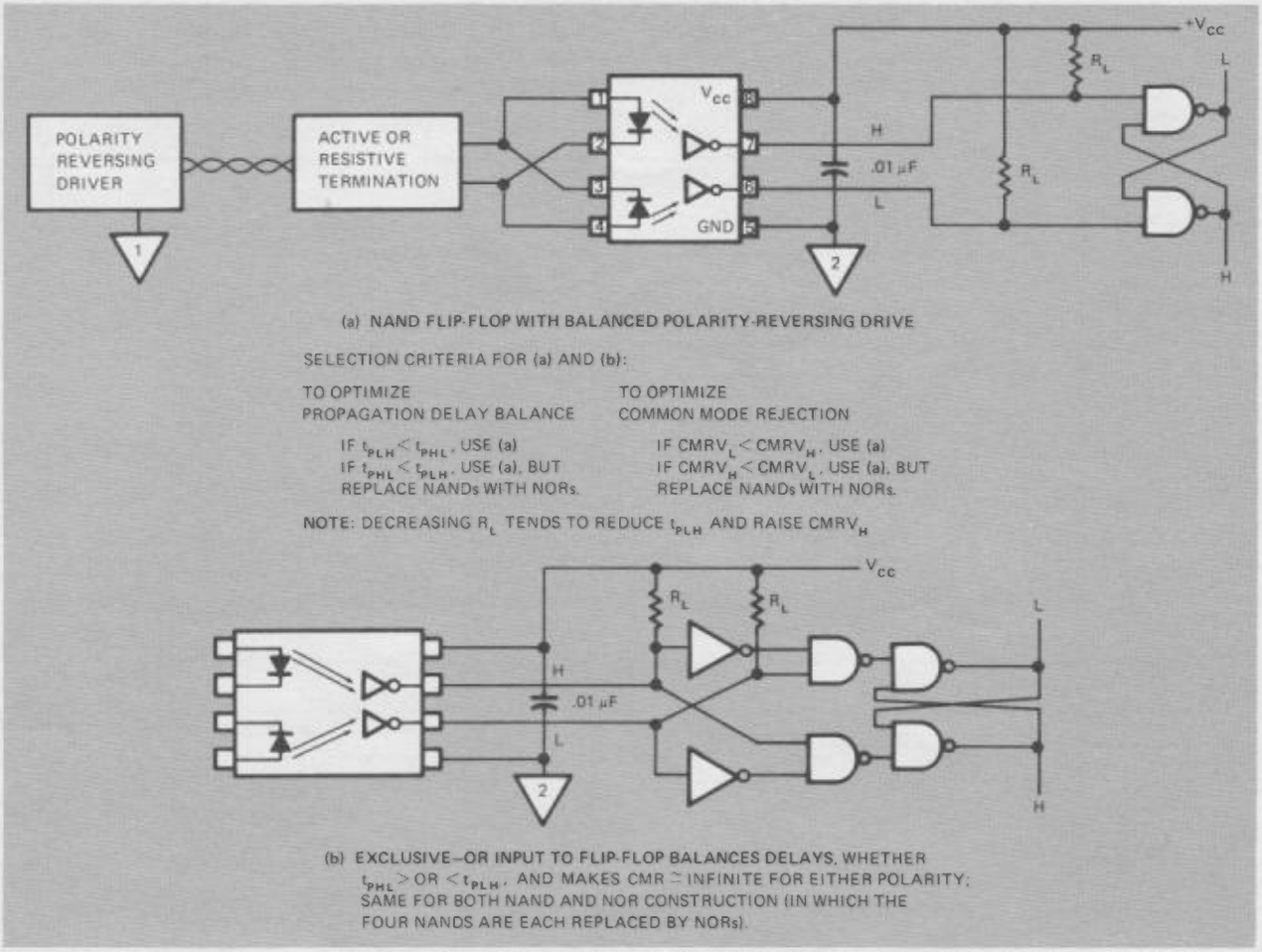


Fig. 6—Balanced resistive terminations can enhance both common-mode rejection (CMR) and propagation delay balance, as well as make threshold adjustment unnecessary. Whenever polarity-reversing drive is employed, the anti-parallel LED used (**Fig. 2**) may be replaced by the input diode of a second (identical) optoisolator to enhance common-mode rejection, balance propagation delay and make threshold adjustment unnecessary.

With respect to threshold and steady-state requirements, the values of R_1 and R_2 in terms of R_3 are found by solving the pair of simultaneous equations obtained by substituting E_{th} for E_T and I_{Fth} for I_F in the circuit equation:

$$\frac{[E_T - (V_F + I_F R_2)]}{(R_1 + R_{DC})} = \frac{(V_F + I_F R_2)}{R_3 + I_F} \qquad (6)$$

where E_T and R_{DC} are found as in **Fig. 7** of **Part 1.** Then, for load matching, obtain R_3 by applying the conditions for CASE 1, CASE 2 or CASE 3. For CASE 1:

$$\left(\frac{V_L}{I_L}\right) = Z_0 = R_1 + \left[\frac{I_F}{(V_F + I_F R_2)} + \frac{1}{R_3}\right]^{-1} \qquad (7)$$

$$\left(\frac{\partial V_L}{\partial I_L}\right)\Big|_{(OFF)} = R_1 + R_3 \leq Z_0 \qquad (8)$$

$$\left(\frac{\partial V_L}{\partial I_L}\right)\Big|_{(ON)} = R_1 + \frac{R_2 R_3}{(R_2 + R_3)} \geq Z_0 \qquad (9)$$

Why not use a dual optoisolator?

Referring back to **Fig. 2** of **Part 2,** we see an anti-parallel LED across the optoisolator. We recommend the LED whenever polarity-reversing drive is used to protect the isolator from excessive reverse bias. However, a superior alternative is to use the input diode of a second identical isolator. In such a design, the two isolators will have balanced, split-phase input currents when a balanced polarity-reversing driver is used. Connect the outputs shown in **Fig. 6** using a NAND (or NOR) flip-flop.

Since the 2-isolator termination is more complex, is it really worth it? A casual look reveals several impressive benefits. Assuming that the isolators are similar, with this design it's unnecessary to perform threshold adjustment to obtain balanced delays. Of course, threshold adjustment may still be worth considering simply to reduce both HL and LH delays. Properly choosing R_L according to the criteria in the figure will give your design the best of two worlds by optimizing both delay balance and CMR. That's a bargain!

Limitations of resistive terminations

A resistive-termination design is simple and economical. But, ah yes, ever since Pandora opened

her box, all good things have had their shortcomings. Resistive terminations have their share of curses, so before you decide they're for your system, know the limitations.

To start, consider the narrow range of applicability—for example, one driver or one cable of fixed length. And when variations among different drivers of the same type number start causing deviations from desired operating levels, you're in trouble. Resistor adjustments then become necessary, slowing down production and increasing the chances for error. The same goes for variations in the length and type of cable.

Worst of all, if the driver characteristics or line resistance ever change from your design values—it makes no difference if the changes are due to changes in production, operating environment or a field change—and you forget just once to adjust the resistor values, any of four curses will plague your system:

1. The receiver will sit inactive when input current drops too low;
2. Or, too much input current will degrade the CTR and sent the optoisolator to an early grave;
3. Delays will become more excessively unbalanced or, if a balanced 2-isolator termination is used, the delays, though balanced, may make your system crawl in slow motion;
4. Those reflections that never affected your longer line may become a scourge when a shorter line is substituted, perhaps years later in a design change.

The only advantages to resistive terminations are freedom from overkill—simplicity and low cost. When you need transmission system flexibility, the best solution is an active termination. □

References

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The fourth article in this 5-part series explores when to use active terminations and explains how to design them. It also will cover CMR enhancement.

Designer's Guide to: Optoisolators—Part 4

When terminating resistors cannot meet data line requirements, use an active termination. Optimizing CMR enhances system performance.

Hans Sorensen, Hewlett Packard, HPA Div.

Active terminations provide many advantages over terminating resistors. Active types regulate the isolator input current with an active element and a feedback path. Because of this, they can adapt the isolator input to driver and transmission line conditions—even when these conditions vary over a broad range.

This article will first address the termination needs when environmental conditions render resistive terminations inadequate. Then we will review how common-mode signals degrade system performance and discuss some methods for enhancing common-mode rejection.

Do you really need an active termination?

The process of choosing between a resistive termination and an active one should be made only after examining system constraints. If the driver, line and isolator will not suffer from wide variations in their characteristics, then resistive

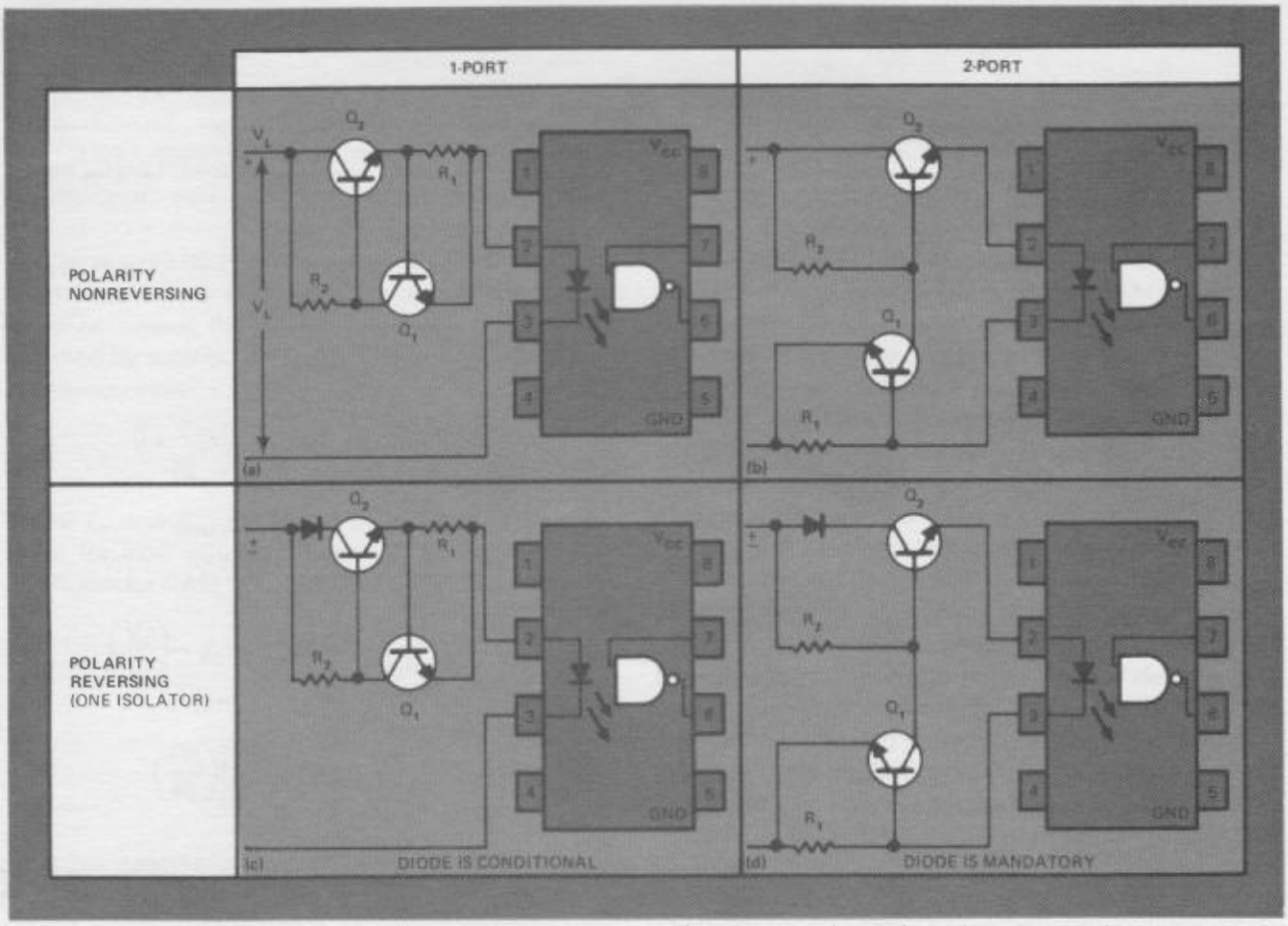

Fig. 1—Current-clamp regulators regulate current flow with a series pass transistor, Q_2, which receives self-biasing current through R_2. With increasing current, the emitter-base voltage on Q_1 increases, causing Q_1 to remove base current from Q_2. The 2-port regulators shunt the incremental current increase across the isolator input and offer improved regulation over that of the one-ports.

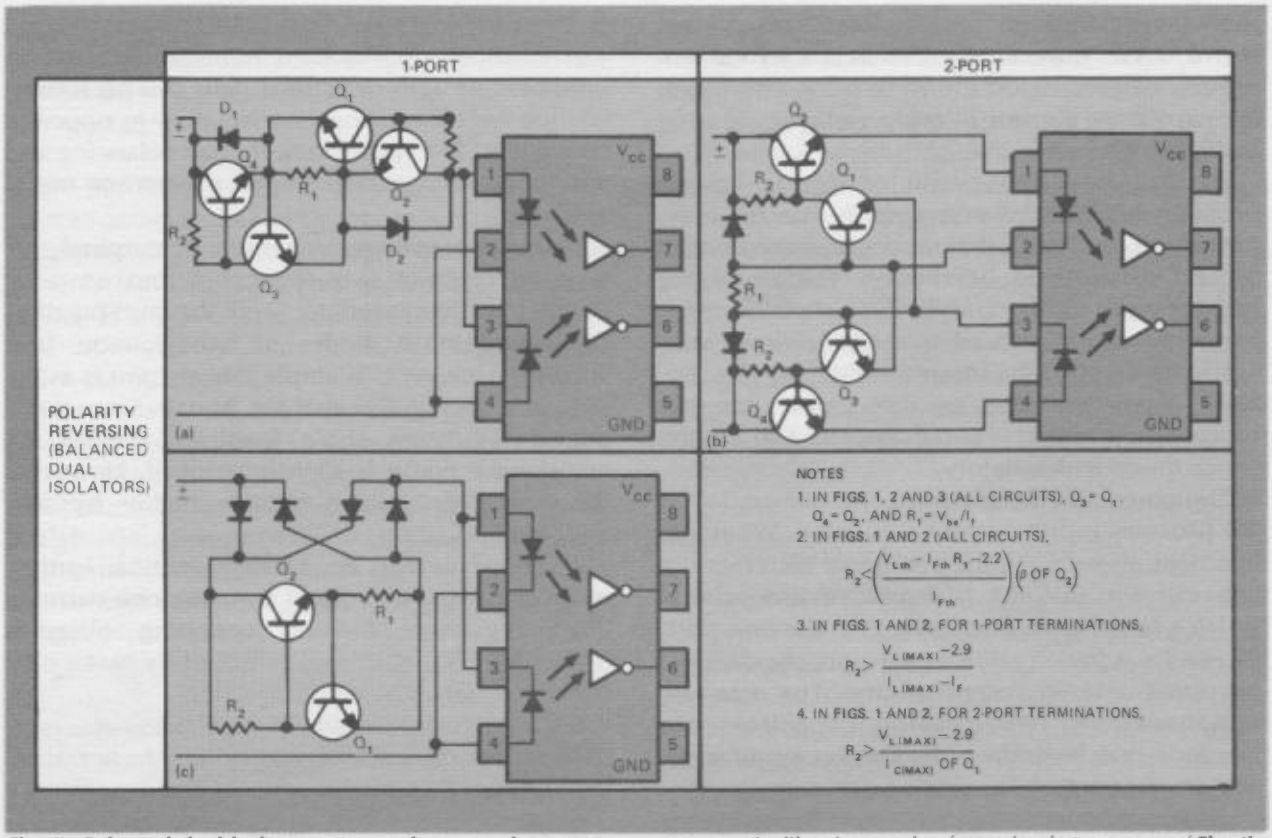

Fig. 2—Balanced dual-isolator, current-clamp regulators provide load balancing when a polarity-reversing driver is used. The 1-port termination **(a)** is merely a combination of two simple one-ports of **Fig. 1a**, but with a common R_1. The two-port is, likewise, made of two simple two-ports of **Fig. 1b**. Bridge regulator **(c)** is a 1-port regulator of **Fig. 1a** across the diode bridge.

terminations provide the most cost-effective solution. Active terminations should be used in the following situations:

- Busing, where changing the number of stations influences the current available to the termination.
- Power supply fluctuations at the driver.
- Changing the length of transmission line, where line resistance is a significant part of the source resistance.
- Temperature changes on long lines ($\Delta R/R \approx 0.4\%/°C$ for copper wire).
- Design flexibility requiring the same termination to be operated by any of several types of drivers.
- Data rate enhancement when a long or lossy line degrades the rise time at the termination.
- Mismatch reflections causing excessive variation in terminal voltage/current.

Although active terminations require higher terminal voltage and data rate for very short, low-loss lines, and cost more, your only concern in an active termination design is proper steady-state ON current. Threshold adjustment becomes unnecessary, since with a voltage-clamp regulator the threshold is lower than for a resistive termination. Load matching can also be neglected because terminal voltage or current variations produced by reflections are attenuated at the regulator, leaving the isolator unaffected. And where reflections must be controlled, a series or shunt resistor added to the active termination will do the trick.

Basically, active terminations fall into two categories: current and voltage-clamp regulators. Both circuits perform current regulation, but the current-clamp regulators let the line voltage rise, while the voltage-clamp regulators allow the line current to rise.

Current regulators provide high dynamic Z

Current-clamp regulators are series-pass circuits. **Figs. 1 a-d** and **2 a-c** show seven different current-clamp regulators. Of these, the first two (**Fig. 1a** and **b**) show most clearly the basic principles on which the other five are based.

The one-port regulator of **Fig. 1a** consists of a series-pass transistor (Q_2), a self-biasing resistor (R_2) and a feedback resistor (R_1). With minimal voltage, Q_2 conducts, receiving base current through R_2. As line voltage rises to $V_F + 2V_{be} \approx 2.9V$, line current becomes high enough so that the voltage drop across R_1 turns Q_1 ON. This, in turn, limits base current to Q_2 by bypassing much of

the current through Q_1. As line voltage rises above 2.9V, only a slight increase in current occurs, depending on the value of R_2. Therefore, line (isolator) current is fairly well regulated at V_{be}/R_1.

The current-clamp circuit of **Fig. 1a** has no problem handling reverse-polarity line drivers—providing, of course, that reverse voltage doesn't exceed the reverse breakdown voltage of the isolator input diode. Should this possibility exist, connect a diode with adequate breakdown voltage in series with the input termination (**Fig. 1c**). Note, however, that in the 2-port polarity-reversing current-clamp regulator of **Fig. 1d,** the series diode is mandatory.

Compared to the one-port, the two-port (**Fig. 1b**) provides better current regulation. When the line rises above 2.9V, the additional increment of line current ($\Delta V_L/R_2$) is bypassed around the isolator rather than through it as in the one-port. R_2 can be a lower value in a 2-port circuit, thus providing a faster response time. For data rate enhancement, two peaking capacitors are needed—one from the collector to emitter of Q_2 and another across R_1.

A 2-way road needs a dual regulator

A balanced dual-isolator termination must be regulated in both directions. This can be accomplished by connecting two isolators in opposite phase (**Fig. 2**) to provide both load balancing and split-phase outputs to improve common-mode rejection.

If the line voltage amplitude is marginal, it's best to connect two regulators into an anti-parallel configuration to feed the anti-parallel-connected input diodes of two isolators (not shown). However, if ample line current is available, use the regulators of **Fig. 2a** or **b**. Since these paired regulators share feedback resistor R_1, component count is slightly reduced. However, the operating voltage is now higher by one additional V_{be}.

As shown in **Fig. 2c**, a bridge rectifier further reduces component count by using one current-clamp regulator. However, operating voltage is higher by 2 V_{be} than that required by previously discussed current-clamp regulators.

Because current-clamp circuits present a high dynamic load resistance, they are better than voltage-clamp types if the line driver has a

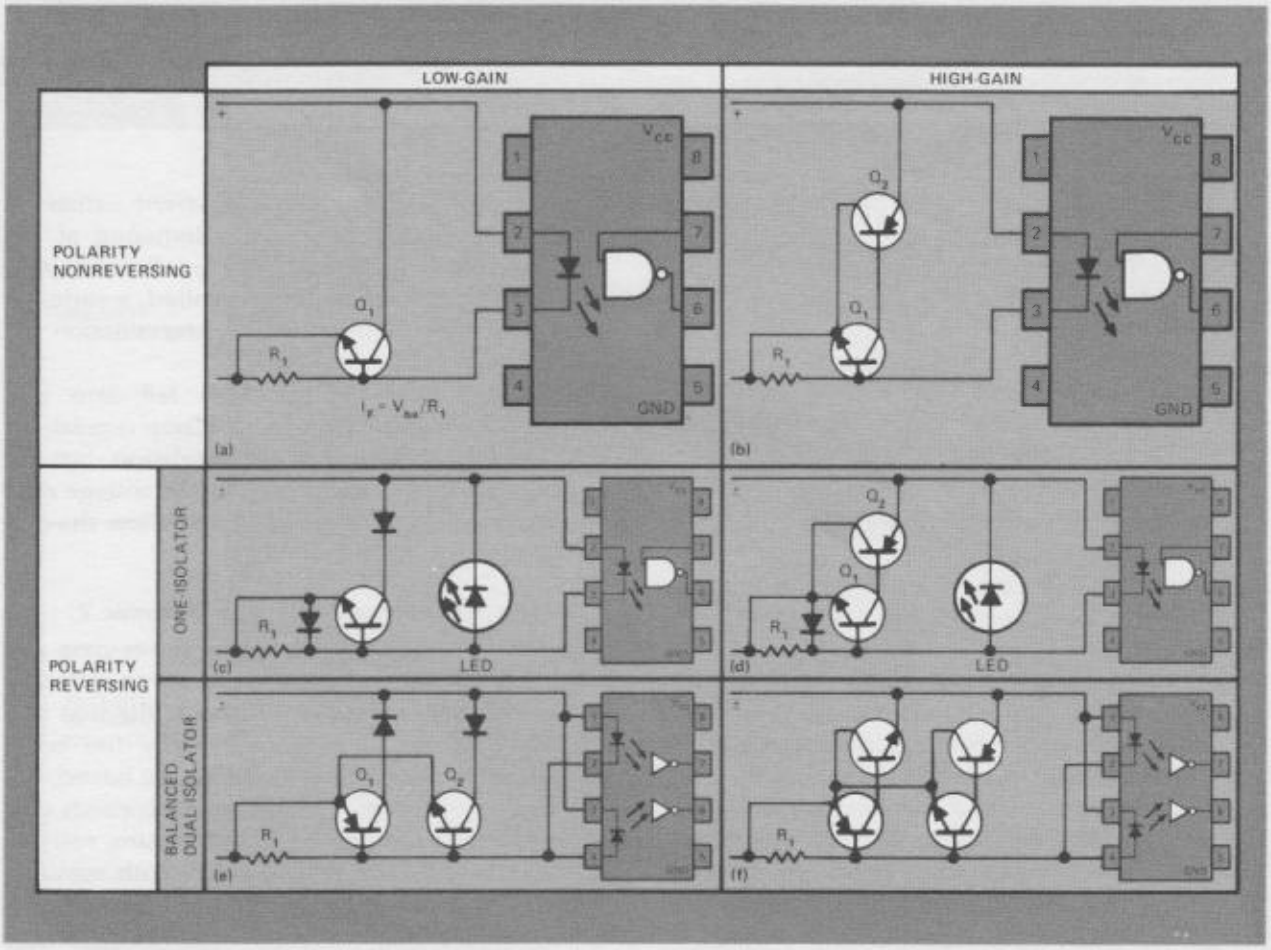

Fig. 3—Voltage-clamp regulators are generally better than current-clamp because of lower turn-ON voltage. The shunt-type regulator maintains constant voltage by conducting more heavily, shunting the excess current across the line. The high-gain circuits on the right provide better regulation than the low-gain terminations. One-isolator circuits (**c** and **d**) use an anti-parallel LED to protect the isolator photodiode from excess reverse voltage.

positive reflection coefficient. As it turns out, such a high-impedance driver makes a low-speed system anyway, and, therefore, response speed is unimportant.

When you need a high-speed regulator...

Of all active terminating circuits, voltage-clamp regulators (**Fig. 3**) are generally better than the current-clamp variety. This is because turn-ON occurs at a lower line voltage of $V_L=V_F$, rather than $V_L=V_F + V_{be}$ or more, as required by series-clamp circuits.

As shown in **Fig. 3a**, the termination begins conducting when line voltage exceeds $V_F \approx 1.5V$. As line current increases beyond V_F, the isolator input current rises until the voltage drop across R_1 is high enough to activate Q_1, which then shunts additional increments of line current, clamps the line voltage at $V_F + V_{be} \approx 2.2V$, and regulates the isolator input current at $I_F = V_{be}/R_1$.

TABLE 1
COMPATIBLE BUSING COMBINATIONS

OPERATING VOLTAGE	POLARITY NONREVERSING	POLARITY REVERSING	
		SINGLE	BALANCED DUAL
$V_F + 4\,V_{be}$			2c
$V_F + 3\,V_{be}$			2a 2b 3e 3f
$V_F + 2\,V_{be}$		1c 1d 3c 3d	
$V_F + V_{be}$	1a 1b 3a 3b		
FIGURE:			

Actually, as line current rises above I_F, some slight increase in line voltage and isolator current will occur, depending on the β of Q_1. However, if this slight increase in line voltage causes inadequate regulation of I_F, the high-gain circuit of **Fig. 3b** should be used. The latter also turns ON at V_F and clamps at $V_F + V_{be}$, but, because of higher gain, regulates better.

With its lower turn-ON voltage, a voltage-clamp regulator performs better than a current-clamp regulator in high-speed operation—and it's not necessary to use a high-speed transistor. Paradoxically, a slow transistor actually permits faster switching. This is because the slower transistor allows a current peak to enter the isolator input until the transistor comes on and regulates the current. These current peaks, of course, must not exceed the maximum ratings of the isolator input diode.

Operation of the reversing, 1-isolator system of **Fig. 3c** and **d** is the same, except in reverse polarity. At this instant, current flows through the LED, thus keeping the reverse-polarity line voltage at a safe level. The collector diode of **Fig. 3c** prevents Q_1 from turning ON in reverse. In **Fig. 3d**, this function is performed by the base-emitter junction of the pnp transistor.

If reverse-polarity line current exceeds the maximum rating of the LED, you should use the circuits of **Fig. 3e** and **f**, substituting a LED for the input of the second isolator. The current in the substitute LED will, of course, be regulated as would the input current of the second isolator.

The previously mentioned active terminations provide good design flexibility when busing enters the picture. **Table 1** shows combinations directly compatible and modifications that permit other busing combinations. The only limit on the number of terminations is set by available line current and voltage.

At this point, let's look at a problem that has given more than one designer many a sleepless night.

How to murder a signal

If your data transmission-line prototype is connected and running, and all your module receives is spurious garbage, common-mode voltage could be the culprit. The differential-mode signal could be drowning in a sea of noise.

Eliminating the effects of common-mode signals is a major task confronting all designers of data transmission lines.

Common-mode interference is sometimes inherent in the system design. More often than not, though, it is incidental. Examples of inherent common-mode signals include:

- Floating equipment with its common point offset from ambient ground. The offset is the common-mode voltage, being common to all points in the floating unit with respect to ambient ground.
- Equipment having a line noise filter. The capacitors in the filter place the chassis at a potential somewhere between the potential of each power line. With one side of the power line at ambient ground (e.g. 115V line), the chassis is offset by approximately 58V. Even if power line voltages are balanced to ground (e.g. 220V line), filter capacitors may not be balanced, thus causing an offset.

Examples of incidental common-mode signals include:

- Offset current coupled through interwinding capacitance of a power transformer.
- Electro-magnetically induced (EMI) interference coupled from equipment or adjacent lines.
- Offset voltages caused by flow of ground-loop currents in the interconnecting wires between modules.

Common-mode voltage in a data transmission system is measured with respect to the common point of the receiving unit's output circuit. The

isolator input diode draws current and produces photons only in response to the differential mode signal. Unfortunately, another effect enters the picture—common-mode capacitance, C_{CM}, which capacitively couples the common-mode signal, e_{CM}, to the base of the output amplifier proportionately to the current flowing in C_{CM}, or: $i_{CM} = C_{CM}\ (de_{CM}/\ dt)$.

Too steep an edge means trouble...

Common-mode rejection (CMR) properties of the isolator are given as rate of change of e_{CM} and

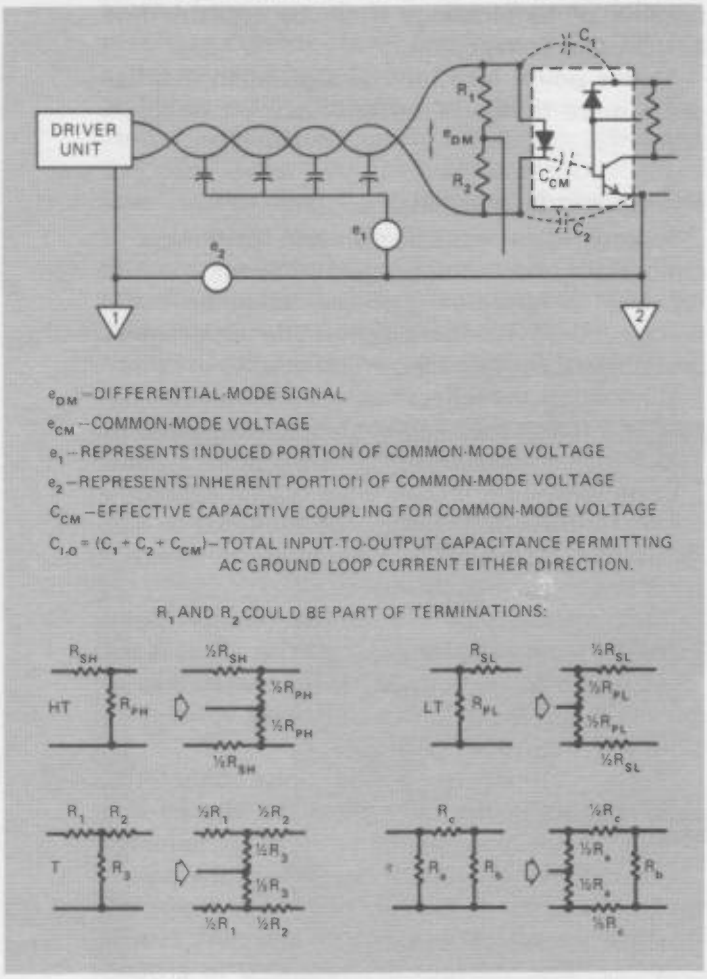

Fig. 4—These arrangements measure common-mode voltage and reduce induced common-mode voltage. Common-mode voltage, e_{CM}, consists of an induced (e_1) and inherent voltage (e_2). A twisted-pair line lowers induced e_{CM}. Since both lines vary simultaneously, no voltage difference should appear at the termination. Inherent e_{CM} can be minimized by good pc-board layout, neutralization and "trick" circuits.

influence the output. As we know, the output should be at a logic HIGH when the differential mode signal, e_{DM}, is in the OFF state, and at a logic LOW when e_{DM} is ON. For each of these two states, a maximum tolerable rate of change of the common-mode signal exists, which, if exceeded, may cause trouble in the form of excessive deviation in the output logic state voltage. This maximum tolerable rate of change determines the CMR property. It is given in either CMRV or CMTR.

Common-mode rejection voltage (CMRV) is the maximum tolerable common-mode ac voltage. But beware of CMRV specs given for only a single frequency, as this invariably gives a false impression of the CMR property. As a function of frequency, CMRV has a slope of −1 on log-log scales, continuing to the cutoff frequency of the output transistor (or amplifier). Beyond the cutoff frequency, the CMRV curve assumes a positive slope.

Common-mode transient rejection (CMTR) describes the maximum tolerable rate of rise (or fall) of transient changes in common-mode voltage and is usually given in volts per microsecond. Positive-going transients tend to turn the output ON when it should be OFF, while negative-going transients tend to turn the output OFF when it should remain ON.

Once again, a false impression of the CMTR property results if CMTR is provided for only one condition of transient amplitude (or duration). The reason is that an arbitrarily high rate of rise (or fall) can be tolerated for a sufficiently small amplitude (or short duration). A curve of $\partial e_{CM}/\partial t$ vs. e_{CM} (for both negative and positive transient slopes) provides a complete description of CMTR.

Tools for enhancing CMR

Methods of reducing the effects of EMI include using a twisted-pair line, a shield, good pc-board layout and "trick" circuits.

A twisted-pair line reduces common-mode voltage by balanced coupling. When e_1 is not coupled equally to both sides of the line, the net unbalance appears as a differential mode signal, as shown in **Fig. 4**. A twisted line pair helps to equalize the coupling of both electric and magnetic EMI. Also, balancing the impedance of each wire to Ground 1 further equalizes coupling.

A shield, unlike the twisted pair, does not balance coupling; instead, it reduces the net unbalance of the coupling e_1 to the lines.

Where would you connect the shield? To Ground 1? If so, you've just made a common mistake. Unfortunately, this won't protect your system, since connecting the shield to Ground 1 is good practice ONLY if the internal impedance to Ground 1 is the same at both output terminals. But since these internal impedances are usually unbalanced, it is a better idea to let the shield float. If not—and if internal impedances are sufficiently unbalanced—a shield connection to Ground 1 may prove worse that no shield at all! So, where should you connect the shield?

To reduce the effects of e_1, the BEST place to

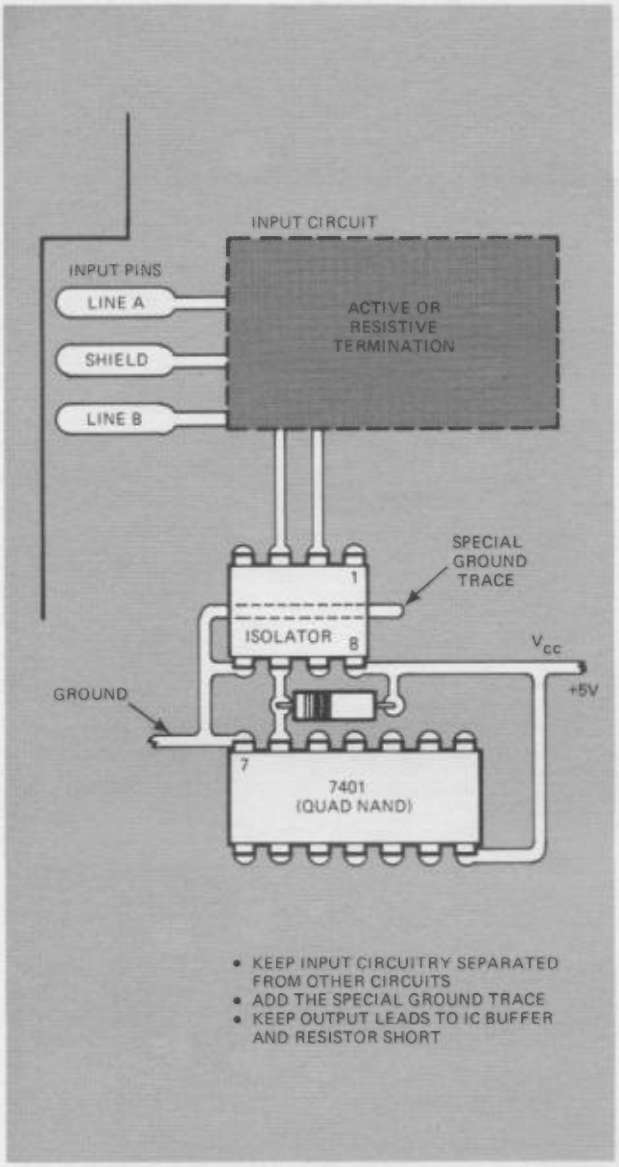

Fig. 5—Circuit board layout can raise common-mode rejection. Input circuitry, obviously, should be separated from all other circuitry. Capacitive coupling between input diode and the transistor base can be lessened by running a ground trace beneath the input and output pins. And, of course, output leads to the IC buffer and resistor should be kept short.

connect the shield is at Ground 2. However, if e_2 is a very high voltage, a shield connected to Ground 2 while the line inside is referred to Ground 1 can cause insulation failure. If e_2 is a high dc voltage, the benefit of a Ground 2 shield connection can be obtained without the insulation-failure hazard by connecting the shield to Ground 2 via a capacitor with a suitable voltage rating.

The NEXT-to-BEST point for shield connection is a tap on a resistance across the line, such as the junction of R_1 and R_2 in **Fig. 4**. R_1 and R_2 may be part of a resistive termination; such line-to-line resistance may be added to an active termination without disrupting its function—providing the resistance is high enough. Usually R_1 and R_2 will be of equal value, but if the common-mode interference coupling is unbalanced, adjust the tap on the resistance ($R_1 + R_2$) to the point at which e_{CM} is smallest.

The following list ranks shield terminations in the above order of their effectiveness against EMI:

BEST

- To Gnd 2 (but may pose insulation hazard).
- To junction of R_1 and R_2 adjusted for minimum e_{CM}.
- To Gnd 1 with balanced source impedance.

MOST PRACTICAL

- To nothing—floating (not connected, either end).
- To junction of $R_1 = R_2$.

WORST

- To Gnd 1 with unbalanced source impedance.

A good board layout is a must. The effect of common-mode voltage (e_{CM}) can be reduced by good layout of the circuit board, as shown in **Fig. 5**. Position all input circuitry as far as possible from all output circuitry. A ground trace between the isolator pin rows helps to direct electric coupling away from the output of the isolator. This ground trace forms a capacitive coupling parallel to C_{CM} and terminates on output ground rather than on the isolator output circuit.

Running a piece of wire across the isolator parallel to the pin rows, connected to output ground at each end, also helps (for the same reason). Last of all, if insulation "creep" distance is critical, insulated wire can be used instead of a ground trace.

Try a trick or two

With an isolator having a single-stage amplifier (transistor or phototransistor) operated with the emitter grounded, the C_{CM} coupling can be neutralized. This trick requires a neutralizing capacitor, C_N, from the input side (anode, cathode or common point) to the collector pin. As seen in **Fig. 4**, the collector current resulting from e_{CM} will be $-\beta C_{CM}(de_{CM}/dt)$, while the current into the collector from the neutralizing capacitor will be $+C_N(de_{CM}/dt)$. Perfect neutralization requires $C_N = \beta C_{CM}$. But, as far as CMR is concerned, approximate neutralization is better than none.

There are other concerns. Adding C_N increases the ac ground-loop current and the insulation of C_M must withstand e_{CM}. If the required value of C_N is small enough, a gimmick can be used. ("Gimmick" is the old-timer's term for a capacitor formed by twisting together two pieces of insulated wire.) Neutralization works best with polarity nonreversing drive, especially if the input diode is prebiased. If polarity reversing drive is used,

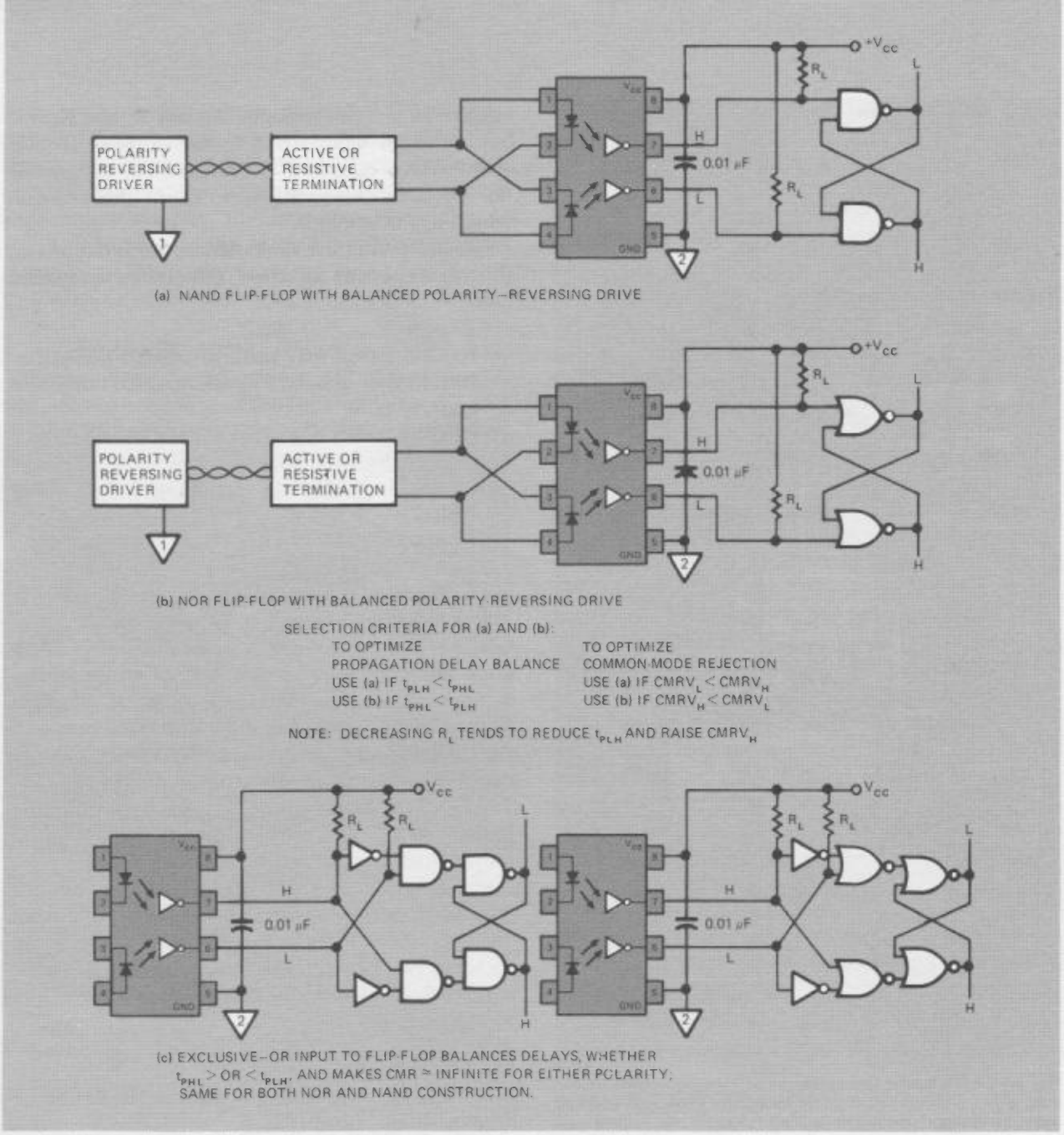

Fig. 6—Output circuit techniques for CMR enhancement. Use **(a)** or **(b)** if isolator properties and/or common mode transcient polarities are known. Use **(c)** for infinite CMR and inherently balanced delays.

other circuit tricks must be considered.

Circuit "tricks" in the output circuit can raise the CMR. They are based on the fact that CMRV and CMTR of the isolator are higher when the output is in the logic LOW state. All such circuits require a pair of isolators driven in split phase, such as with a reversing-polarity driver.

When a NOR-gate R-S flip-flop (**Fig. 6b**) has been triggered by a logic HIGH at one of its inputs, then the outputs (both of them) are immune to any subsequent changes. Since the isolator is more likely to hold a LOW in the face of interference, the NOR-gate flip-flop enhances the CMR of such a pair. This is true because common-mode transients produce output transients of the same phase on each side, whereas a flip-flop requires opposite-phase inputs. As a result, these opposite-phase inputs occur only in response to the desired differential-mode signal.

Another benefit of using a flip-flop output is that the delay times to logic HIGH and to logic LOW are equalized to the extent that both isolators have the same t_{PLH}. Given two isolators with the same drive conditions, it's more likely that t_{PLH} (of #1) = t_{PLH} (of #2) than it is that t_{PLH} = t_{PHL} of either of them.

The choice of NAND or NOR construction (**Fig. 6**) depends on the propagation delay and CMR properties of the isolator, along with the input requirements of R-S flip-flops. In a NAND flip-

flop, simultaneous HIGH inputs are of no concern. However simultaneous LOW inputs will drive both inputs HIGH, a condition to be avoided. Conversely, in a NOR flip-flop, simultaneous LOW inputs are tolerable, while simultaneous HIGH inputs drive both outputs LOW and should be avoided. With a balanced dual-isolator termination, if $t_{PLH}<t_{PHL}$, the NAND flip-flop should be used, with propagating delays balanced at t_{PHL}. This is because the isolator outputs cannot be simultaneously LOW. If $t_{PHL}<t_{PLH}$, the isolator outputs cannot be simultaneously HIGH, so the NOR flip-flop should be used and propagation delays balanced at t_{PLH}.

A final word on common-mode rejection

The isolator outputs will be simultaneously HIGH if $e_{CM}>CMRV_L$ and simultaneously LOW if $e_{CM}>CMRV_H$. For isolators with $CMRV_L<CMRV_H$, the NAND flip-flop is preferred because it can tolerate the simultaneous HIGH's occurring at $e_{CM}>CMRV_L$. Should e_{CM} exceed $CMRV_H$, the resulting simultaneous LOW's at the NAND flip-flop inputs will drive both outputs HIGH. However, when e_{CM} drops, they will return to the proper states as required by the differential mode signal on the transmission line. As might be expected, the improper logic state caused by a common-mode transient is only momentary.

For isolators with $CMRV_H<CMRV_L$, a NOR flip-flop is better (except for polarity). The reason is the same as before, since the improper logic state resulting from excessive e_{CM} is momentary.

These momentary improper logic states can be prevented by adding exclusive-OR logic to the inputs of the flip-flop as shown in **Fig. 6c**. Moreover, the exclusive-OR-ed flip-flop will automatically balance propagation delays. As far as CMR and delay balance are concerned, it makes absolutely no difference whether NOR or NAND gates are used. Keep in mind that if a NAND flip-flop is used, the exclusive-OR-ing must be done with NAND gates; and for a NOR flip-flop, with NOR gates. □

The next and final article will explore data rate enhancement and multiplexing.

Reference

1. Sorensen, Hans, "Opto-isolator developments are making your design chores simpler," EDN, December 20, 1973.

Designer's Guide to: Optoisolators—Part 5

Here are several powerful techniques that increase data rates and open new horizons in multiplexing. How many can you use?

Hans Sorensen, Hewlett-Packard, HPA Div.

When data rate is slower that it should be, the culprit can be the driver, the transmission line or the receiver. Generally, the driver is not a serious limitation, therefore we will ignore it. The line will delay the arrival of the data, but aside from degrading rise/fall times, it cannot affect the data rate. The receiver, however, is where the action takes place, and a poor design here can seriously degrade data rate. This article will offer several solutions to the problem of data rate degradation.

How are your thresholds?

Threshold adjustment was already discussed in **Part 4**. As you recall, balanced thresholds are desirable because they maintain equal time delays and prevent time-distortion of data pulses. Threshold adjustment also can enhance data rate.

Fig. 2 of this part shows how to use threshold offset. The shield of a twisted-pair shielded cable carries the offset voltage from driver to terminal. Even if the offset voltage E_C equals zero, the shield return connection is still beneficial. This is because the line-to-ground voltage for logic HIGH exceeds line-to-line voltage, thereby lowering the threshold (as compared to the steady-state terminal voltage). The termination becomes more vulnerable to common-mode voltage whenever a shield return connection is used—especially if $E_C > 0$. Therefore be sure to use an exclusive-OR-ed flip-flop output circuit.

If a single isolator and polarity-reversing drive are used in the termination, then delay balance is obtained only if negative offset is introduced as in **Fig. 1a**. Also, if the drive is nonreversing, a proper choice of resistors in a 2-resistor HT or LT circuit will balance delays.

With paired isolators (**Fig. 6, Part 4**), balancing is not a problem. However, if you are seeking the maximum in data rate, adjust the threshold for each side of the pair. To see this, compare the delays in **Fig. 1b** with those of **Fig. 1c**, where offset is applied, and with **Fig. 1d**, where peaking is used.

When line-to-line voltage is polarity reversing,

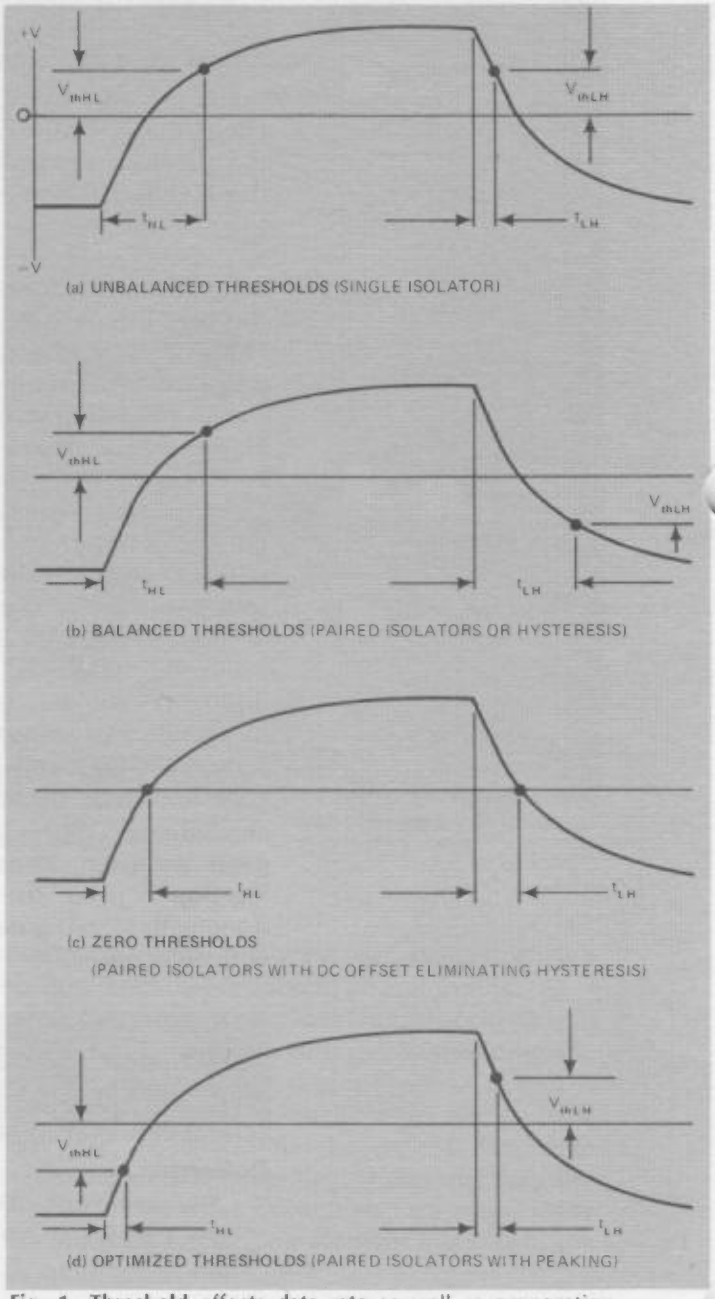

Fig. 1—Threshold affects data rate as well as propagation delay. When $V_{thHL} = V_{thLH} > 0$, the delays cannot be equal (**a**); while if $V_{thHL} = -V_{thLH} > 0$, the delays will balance (**b**). For $V_{thHL} = -V_{thLH} = 0$, the delays will also balance (**c**). Notice the location of the thresholds (**d**) when $V_{thHL} = -V_{thLH} < 0$.

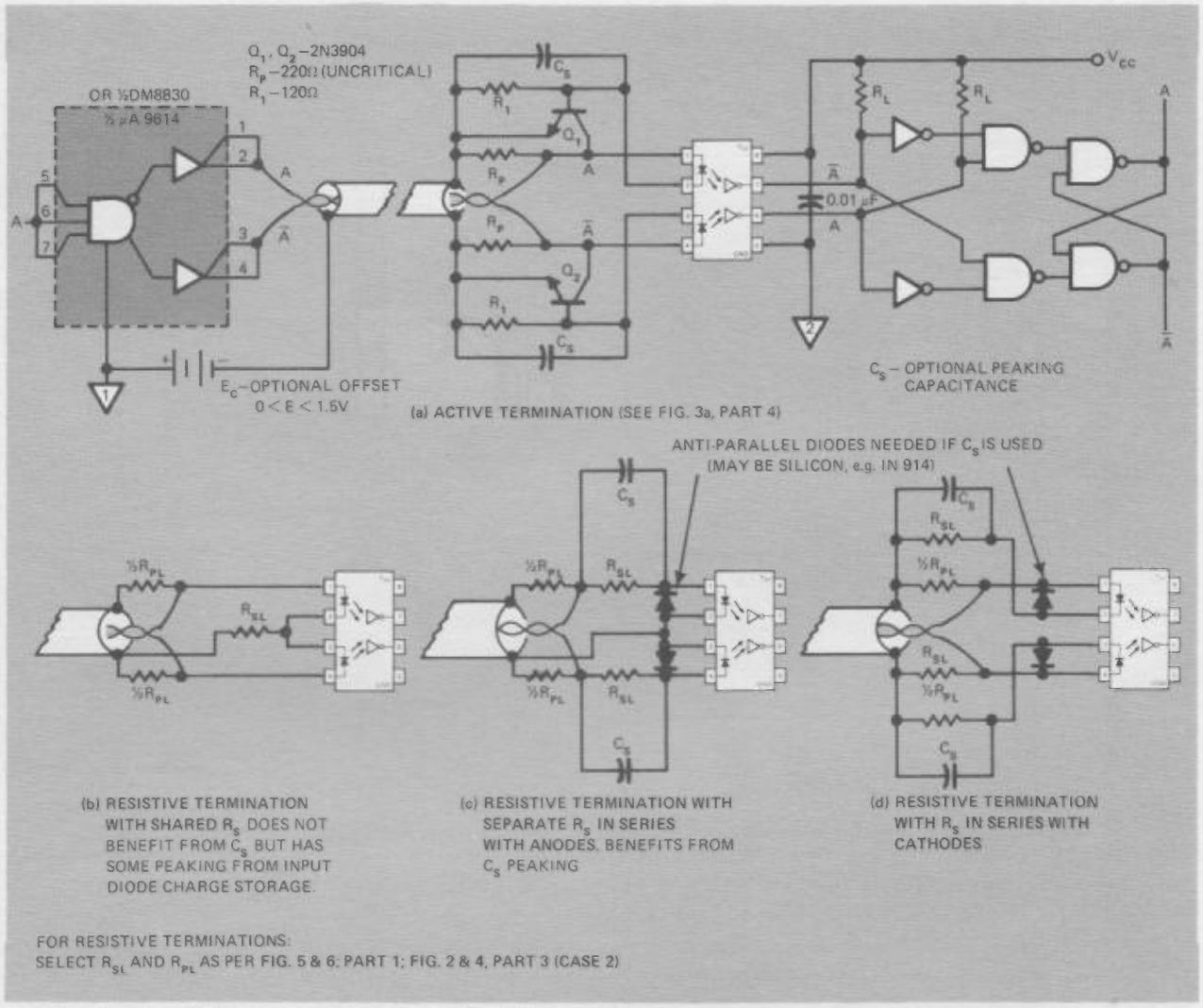

Fig. 2—Using the shield return allows offset for the isolator inputs.

termination of each side of the line to the shield can be a single-ended, polarity-nonreversing design. This is because the line-to-shield voltages are split-phase polarity nonreversing. For the active termination of **Fig. 2a**, the two diodes that handle polarity reversal are eliminated. The termination consists merely of two shunt-pass active terminations for each line.

The same concept of threshold adjustment applies to resistive terminations (**Fig. 2b, c, d**). Find R_{SL} by applying Case 2 (**Fig. 2** and **4, Part 3**), where Z_0 is Z_{otm} as seen in **Fig. 6, Part 1**.

Peaking—the key to isolator speed

The delay involved in turning on the output transistor, t_{PHL}, can be shortened by driving the input diode at a higher current. This forces a higher photocurrent into the isolator amplifier input.

To shorten the delay involved in turning off the output transistor, t_{PLH}, quickly turn off the input diode and wait for the transistor to turn-off. The time required for turn-off depends on how hard the transistor was turned on, so shortening t_{PHL} lengthens t_{PLH}, unless the higher drive current used in shortening t_{PHL} is only momentary. This "peaking" technique increases data rate by providing a momentary surge of forward current during turn-on, reducing to a minimum the acceptable forward current in the steady state. A high momentary forward current is produced by a transmission line with a low characteristic impedance and a low driver internal resistance. Back matching will prove unnecessary if you use the terminations suggested here.

Can peaking affect threshold?

If the high-state and low-state voltage drops across a current-limiting resistance are significantly different, connecting a capacitor (C_S) in parallel with the current-limiting resistance gives peaking. This peaking effect is a threshold shift (**Fig. 3**).

When V_I is negative, the input voltage becomes

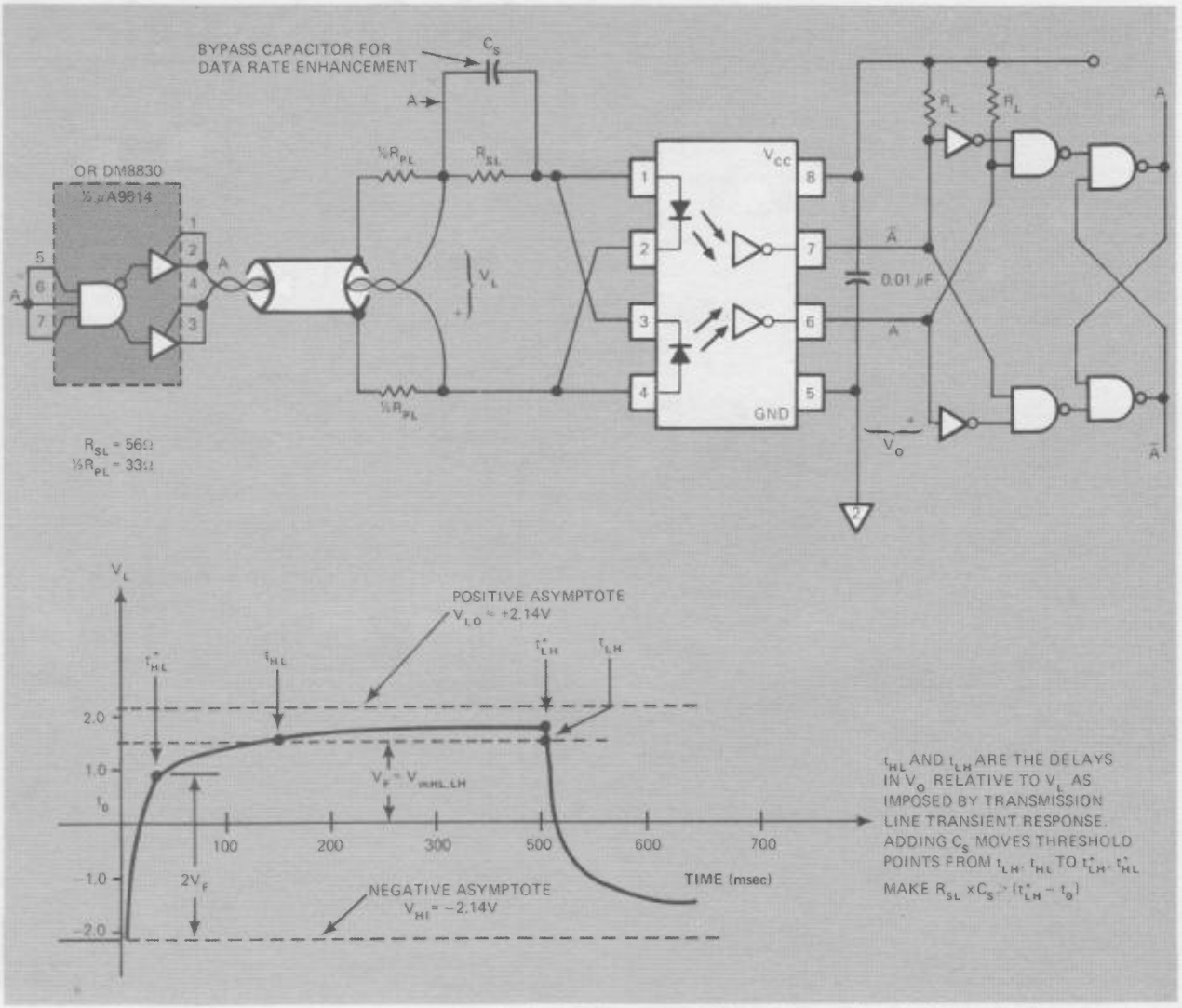

Fig. 3—Peaking capacitor, C_S, increases data rate in a balanced data transmission system with resistive termination.

$-V_F$. Without peaking, V_L rises from its asymptotic negative value to +1.5V before the lower isolator can begin to turn on. On the other hand, with a peaking capacitor, turn-on begins when voltage across the lower isolator input changes from $-V_F$ to $+V_F$. Note that C_S should be large enough so that its voltage does not change very much during the interval (t_{HL}-t_0). The effect of peaking in this case is to shorten t_{HL}.

Without the peaking capacitor, turn-off begins only when V_L drops to the threshold. But with a peaking capacitor, turn-off begins as soon as V_L drops. Because this makes the termination more vulnerable to negative common-mode transients, we recommend an exclusive-OR-ed flip-flop for the output circuits.

Enter "resistive peaking"

As we saw in **Part 2**, a peaking capacitor paralleled with the series resistor of any resistive termination causes a momentary forward-current surge. Unfortunately, this, in turn, can cause oscillatory re-reflections from the driver when you use the simple series circuit (**Fig. 2b, Part 2**), or the HT and LT terminations for threshold adjustment (**Fig. 3, Part 2**).

If Case 2 (**Part 3**) is applied, the 3-resistor π or T circuit can be used. But it makes no sense to design a π or T for threshold and load match and then to upset both with a peaking capacitor. That leaves the HT and LT terminations designed for load matching Case 2 (**Fig. 2** and **Figs. 1-4, Part 3**). Of these, LT terminations benefit most from peaking.

One exception is the circuit of **Fig. 2b**. Here the current in R_{SL} has the same polarity for both logic states. As a result, insufficient voltage change exists for a peaking capacitor in parallel with the resistor to be effective. Still, this circuit has some peaking. During steady state, the ON input diode has a charge stored in it—the charge necessary to support I_F. Thus, when the line-to-line voltage

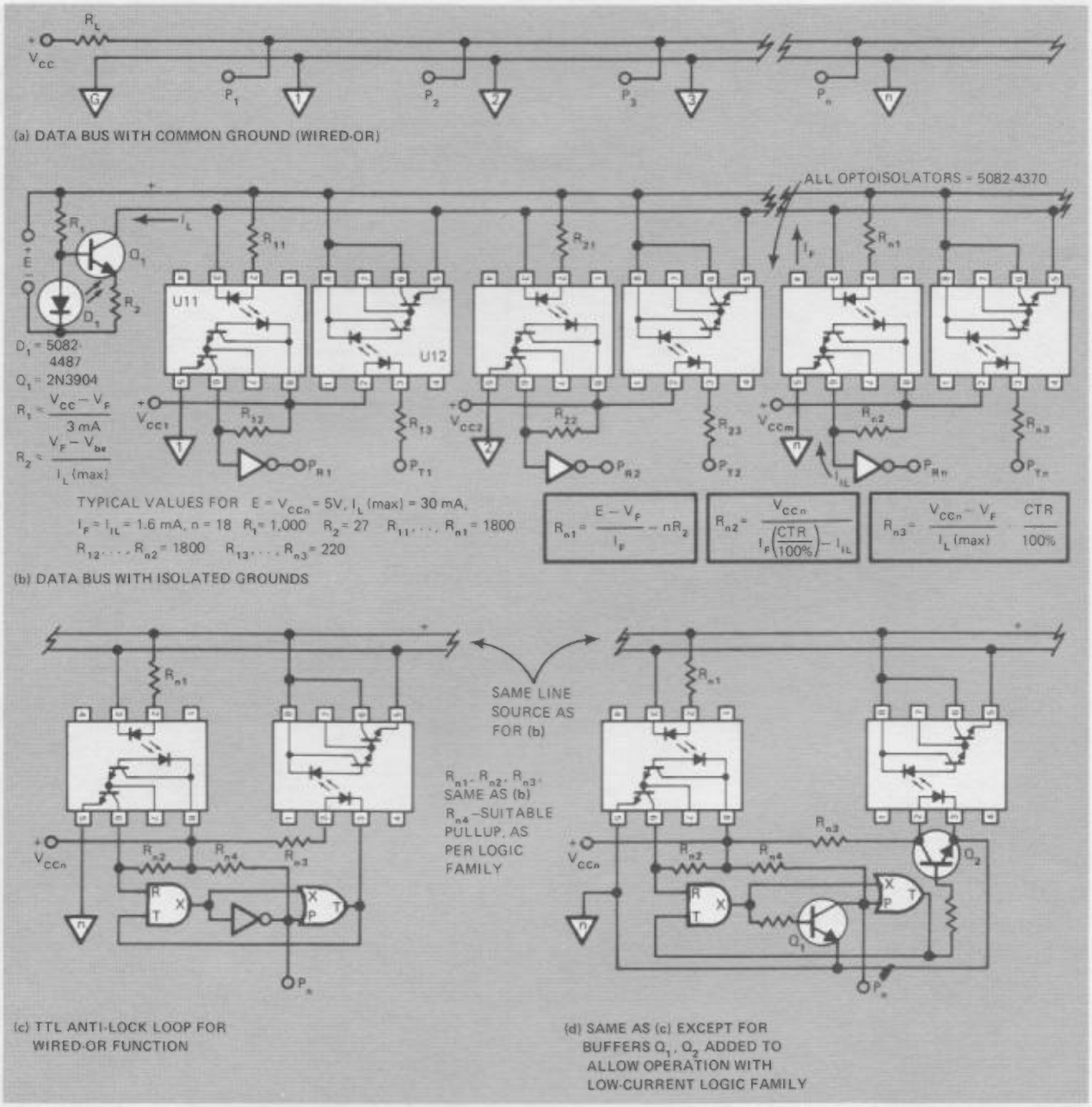

Fig. 4—Moderate data rate multiplexing with high CTR optoisolators is shown. The data bus with isolated grounds **(b)** has separate terminals at each station for receiving (P_R) and transmitting (P_T). The same terminal in each station of the TTL anti-lock loop **(c)** can transmit and receive.

reverses polarity, this stored charge is transferred to the other diode, thereby reducing its turn-on time.

What is the best value for the peaking capacitor? That depends on the shape of the turn-on transient, so a specific formula doesn't exist. Peaking capacitance for polarity-nonreversing drive should be a good deal larger than that required in polarity-reversing drive. Anti-parallel diodes allow C_S to charge and discharge, even if polarity is nonreversing.

To obtain the greatest benefits from peaking, try the circuit in **Fig. 3**, where the polarity on the peaking capacitor is reversed. Peaking capacitance is optional in **Fig. 2**, where the main data rate enhancement comes from threshold control. In particular, since polarity on the peaking capacitor in **Fig. 2c** and **2d** is not reversed, C_S is of little incremental value.

A refresher on active peaking

The voltage-clamp regulators of **Fig. 3, Part 4**, lag line voltage, thereby allowing a momentary surge into the isolator diode. On turn-off, the shunt transistor lags again, remaining on briefly. This helps to drain the charge from the isolator

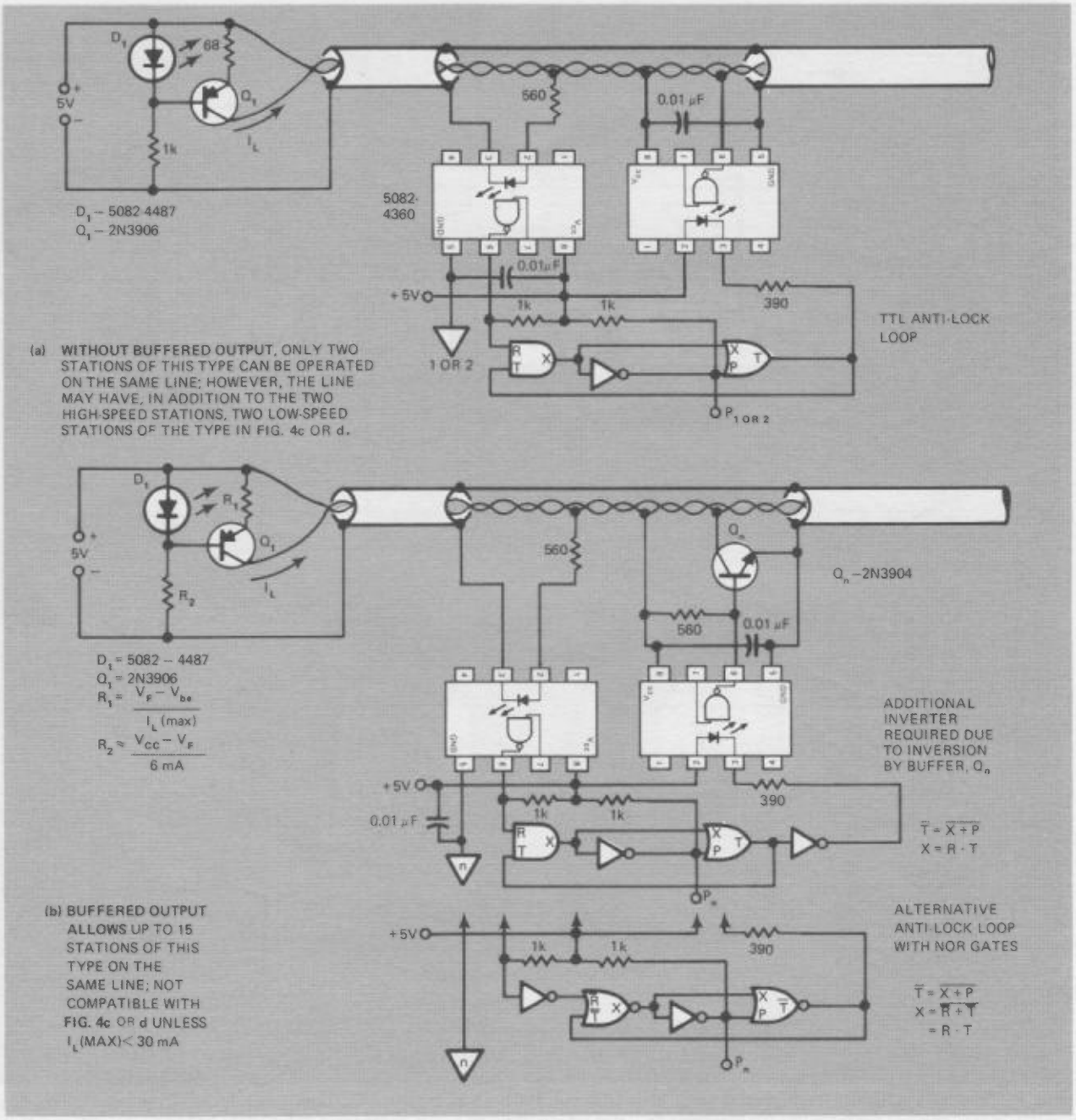

Fig. 5—Data bus multiplexing using high-speed optoisolators with an unbuffered output (**a**) can have only two stations on the line. With a buffered output, up to 15 stations can be hung on the same bus.

diode, thus hastening turn-off.

To further enhance both effects (especially in **Fig. 3 c-f, Part 4**, where voltage across R_1 reverses polarity), place a capacitor in parallel with R_1.

For the one-port, current clamp terminations shown in **Part 4**, you should connect a peaking capacitor in parallel with the entire regulator. Two-port regulators, on the other hand, need more than one peaking capacitor and should have a capacitor in parallel with R_1. In addition, circuits of **Fig. 1b** and **d**, **Part 4** should have a capacitor from the input diode anode to the + or the ± line terminal. The circuit given in **Fig. 2b, Part 4** should have two additional capacitors—one from each input diode anode to the collector of its regulating transistor.

Multiplexing—how optoisolators fit

Data goes only in one direction on a simplex data transmission line, from one driver to one or more receivers. In multiplexing, however, data exchanges in both directions from any of several stations on the line to all other receivers on the line.

Bused multiplexing, as shown in **Fig. 4a,** is a wired-OR arrangement. Each of the terminal

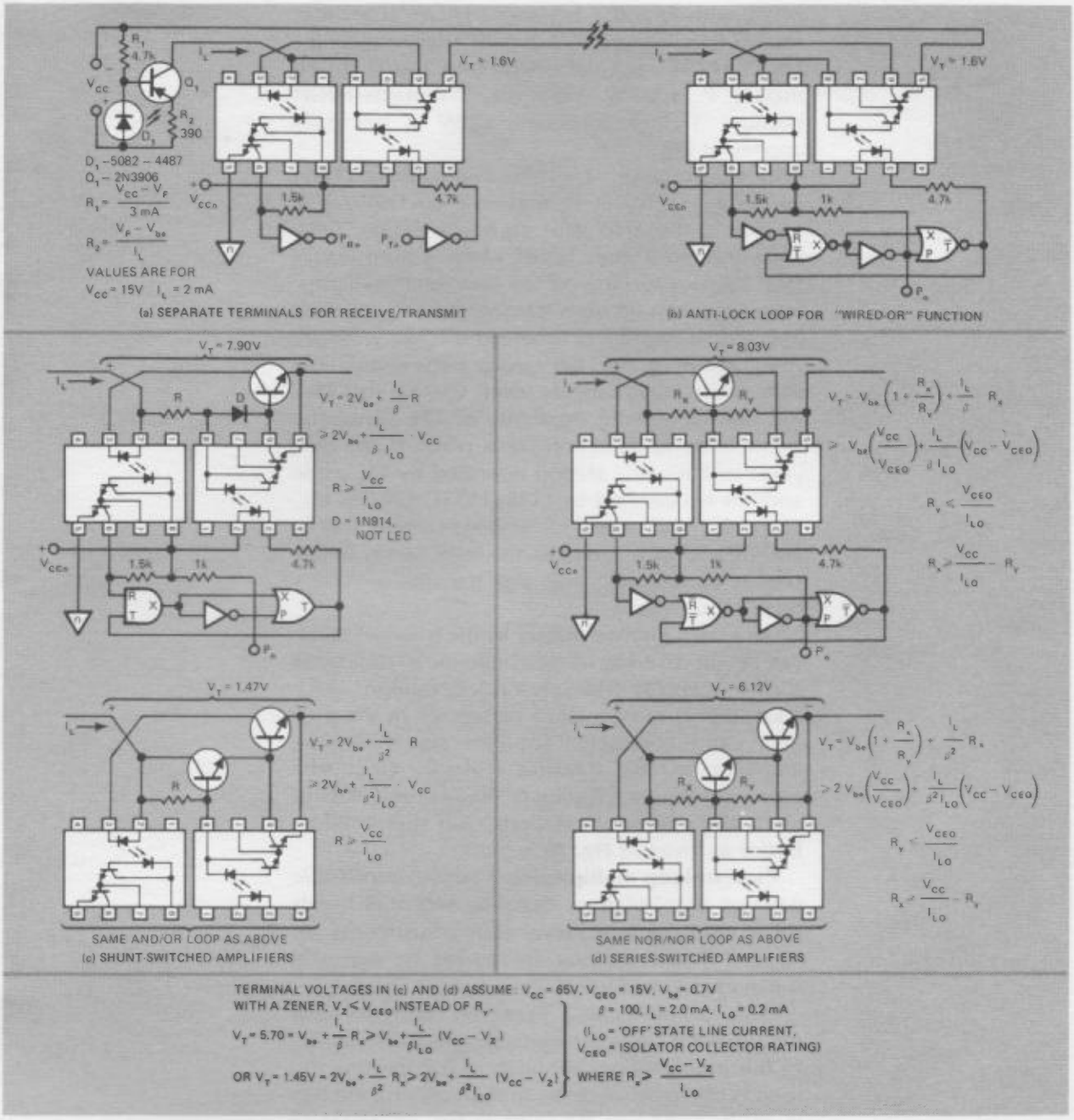

Fig. 6—Current loop multiplexing, otherwise difficult to utilize, poses no serious problems for the designer when optoisolators are used.

points (P_1, P_2...P_n) are at a quiescent HIGH state. Since the transmitter/receivers share a common ground and V_{CC}, applying a LOW at any point causes a LOW to appear at all others.

Ground looping can create common-mode interference and may require that these common connections be separated as shown in **Fig. 4b**. Here one isolator is the transmitter; the other, a receiver. When a LOW is applied to P_{Tn}, the transmitting isolator drops the line voltage by sinking all the current available from the line source. This causes all receiving points (P_{R1}, P_{R2},...P_{Rn}) to go LOW. This differs from the arrangement of **Fig. 4a** because in **4b** the transmit and receive points (P_{Tn} and P_{Rn}) at each station are not common. Though the logic is the same, these points cannot be connected without locking everything LOW.

You can obtain common transmit/receive points by using the AND/OR anti-lock loop shown in **Fig. 4c** (for TTL). The loop requires an open-collector inverter, whose input remains LOW even when a LOW is applied at P_n, thereby ensuring that its output will go HIGH when the LOW is removed from P_n.

In the quiescent state, R is LOW, making X

LOW, with P_n and T becoming HIGH. If another station transmits a LOW, R goes HIGH, causing a HIGH, HIGH input at the AND gate. X goes HIGH, making P_n a LOW. However, T remains HIGH because $T=X+\overline{X}$ (unless a LOW is internally applied at P_n).

In transmitting, $T=X+P_n$. Since X is LOW, applying a LOW at P_n makes T go LOW. T is applied at the AND gate, so X will remain LOW, even though R goes HIGH when T drops LOW (and thereby turning on the "transmit" isolator). Since data can be both transmitted and received at P_n, the wired-OR is achieved.

The anti-loop (**Fig. 4d**) can be made compatible with other logic families (even CMOS) that lack the current-sinking capability of TTL. Since the isolated interconnection takes place at the bus, you can have one station operated by TTL while another is operated by LTTL, LSTTL, CMOS, etc. The only requirement for isolated wired-OR is an anti-lock loop that makes the logic family in any station compatible with the transmit isolator's drive requirement.

Data rates, limited mainly by the isolators used, can be improved by using a high-speed isolator as shown in **Fig. 5a**. There is a price, though, and it takes the form of a third connector in the bus. This extra connector supplies power to the amplifier in the transmit isolator. Since the current-sinking capability of the transmit isolator limits the number of stations, you should add a buffer as given in **Fig. 5b**.

Current-loop multiplexing is next to impossible without optoisolators. Because potential builds up around the loop, level shift adjustments are needed when stations are added or removed (unless relays are used).

With optoisolators, however, current loop multiplexing becomes quite simple and is similar to bus multiplexing, although in transmitting the loop is opened; whereas, in multiplexing the bus is shorted. As can be seen in **Fig. 6a**, separate transmit and receive points can be used at each station. If a common transmit/receive point is needed, you must use the anti-lock loop (**Fig. 6b**).

The voltage rating on the isolator collector limits the number of stations in a current loop. To increase the number of stations, it may prove necessary to raise the voltage rating by using circuits such as **Fig. 6c** or **d**. □

This fifth and final article concludes EDN's optoisolator digital transmission line series.

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