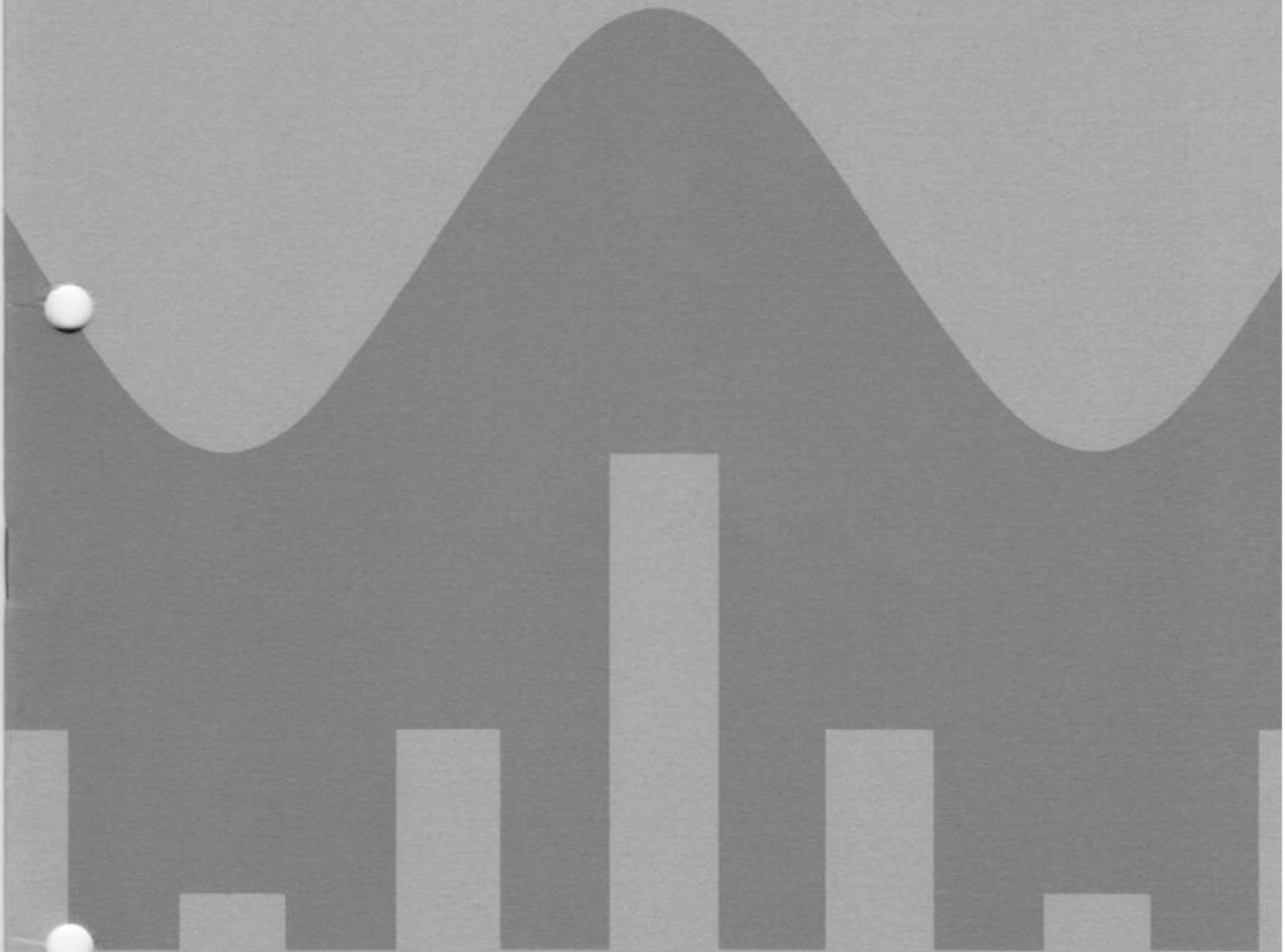
Telecommunication Measurements and the PMA

Single Channel Codec Testing

AN 231-1



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Introduction

Today the world, and in particular the telecommunications industry, is adopting digital techniques. For transmission and switching, digital technology allows the demand for growth and improved services to be accommodated economically. Large integrated digital systems are being installed in many countries with a view to extending the digital interface out to the customers' handsets. The present public telephone system has in excess of 450 million terminals, and as each requires conversion to work with the new systems, the potential demand of the terminal manufacturer for codecs is tremendous.

What is a Codec?

To enable voice frequencies to be converted to binary digits (the process of enCODing) and the binary digits to be reconverted back to voice frequencies (the process of DECoding) a device known as a CODEC is used. The binary digits encountered with codecs are generally in a PCM format conforming to one of two internationally recognised standards:

(a) The CEPT system to CCITT Recommendations G.711 and G.732, with a transmission rate of 2.048 Mb/s.

(b) The BELL system to CCITT Recommendations G.711 and G.733, with a transmission rate of 1.544 Mb/s.

However, for a single voice channel only 64 kb/s is required with either of these standards (8 kHz sampling and 8 bits/sample encoding).

The transfer characteristics for the codec are internationally standardized as either μ-255 law for the BELL system, or A-law for the CEPT system. Up to now the codec has been common to a number of multiplexed channels, but flexibility and the desire to extend the digital interface to the customer has spurred the economic design of smaller module codecs, either on a per channel or dual basis. These codecs may be LSI or discrete, in component form or supplied as part of a line interface unit.

Most major semiconductor manufacturers have recognised the need for LSI designs for the codec and its associated circuitry, and have produced or are about to produce a codec on a 'chip'. Associated with each codec is the need for filtering – at the encoder to limit spurious inputs, and at the decoder to reconstruct the analog outputs. Codec manufacturers have responded with a number of alternatives; for example, the encoder and decoder may be on a single chip, or filter and encoder may be one chip with decoder and reconstruction filter (often referred to as a $\frac{\sin X}{X}$ filter) on another. Incorporated on these chips are facilities such as built-in auto-zeroing, power-down capability, synchronous or asynchronous operation, and the ability to handle serial data rates of 56 to 3152 kHz at 8 kHz nominal sampling rate. A wide range of fabrication technologies exists but manufacturers have settled on either NMOS, CMOS, or I^2L, mostly with TTL-compatible interfaces.

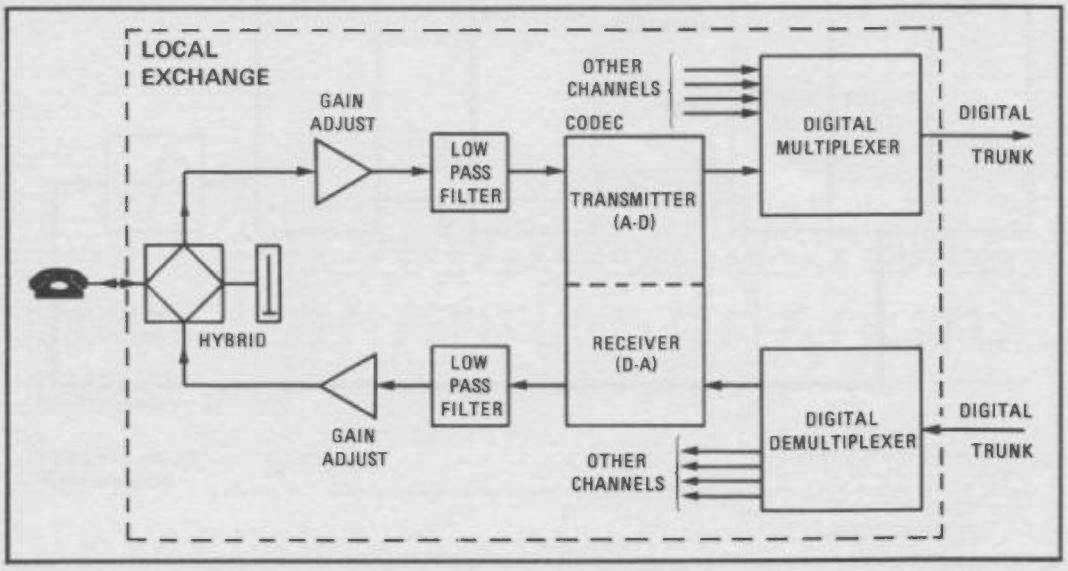


Figure 1 The Codec Function

The Role of the PMA in Codec Testing

The HP 3779 Primary Multiplex Analyzer (PMA) can make the measurements called for in CCITT Recommendation G.712 on an analog-to-analog (A-A) basis, and also enables the separate characterization of both encoding and decoding by making analog-to-digital (A-D) and digital-to-analog (D-A) tests. A-D and D-A single channel measurements are conducted through a single channel interface connector on the rear panel of the PMA.

In view of the many possible codec designs now being produced, with no standardized interface agreed, the PMA has been equipped with a general purpose TTL-compatible interface. This enables a simple digital interface to be constructed to connect the PMA to the codec (see Figure 2).

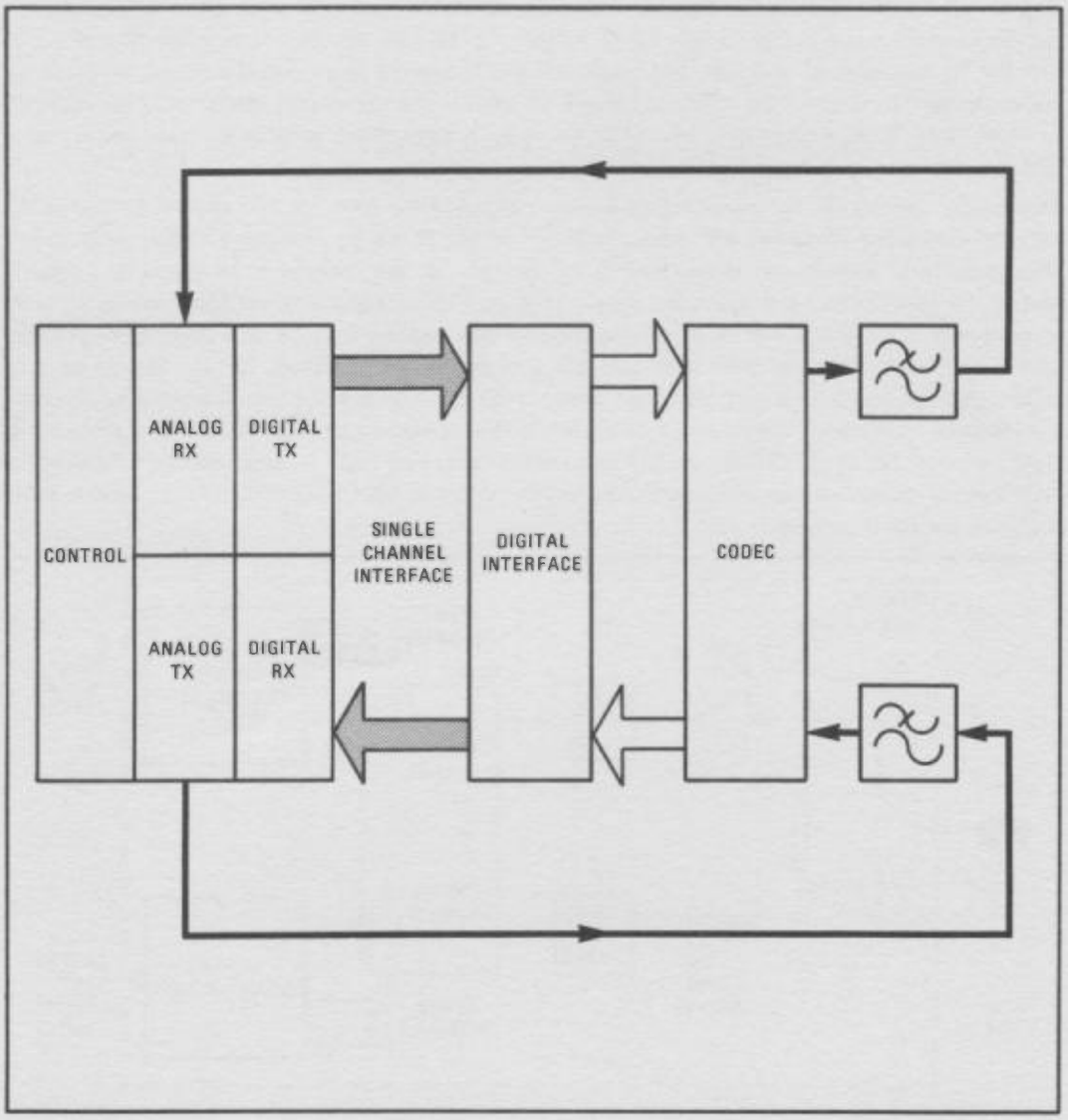


Figure 2 Single Channel Codec Testing

Interfacing the PMA & a Single Channel Codec

The single channel data may be in serial or parallel format, and consist of one 8-bit word for each frame of digital transmitter/receiver operation. In serial format, the eight received bits may occur at any clock intervals within the frame. (For example, they may be bunched together over eight successive clock periods, or they may be spaced over a one-frame period). Timing relationships for both serial and parallel operation are shown in Figure 3.

The single channel outputs from the PMA are delivered from open collector TTL buffers in 'low true' format. The output word is identified by a low true data valid signal. Serial or parallel working is selected internally via a link on the A17 card in the PMA.

The single channel inputs to the PMA are accepted at 125 μs intervals. Each 8-bit word, serial or parallel, drives a schmitt trigger buffer inside the PMA designed for open collector TTL inputs in 'low true' format. The input must be accompanied by a low true data valid signal and a clocking signal.

Since most codecs require a clock for their transmit half to function, a PMA clock is available at 2048 kHz (HP 3779A) or 1544 kHz (HP 3779B).

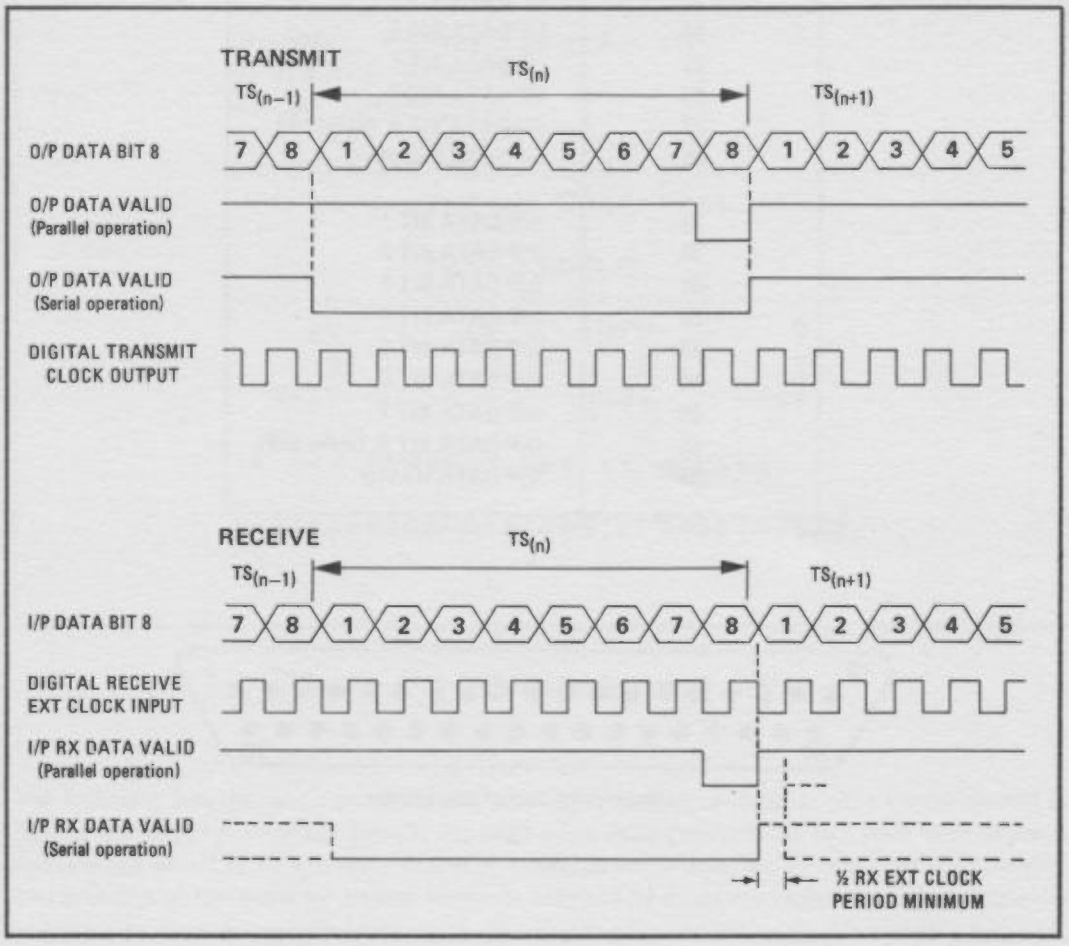
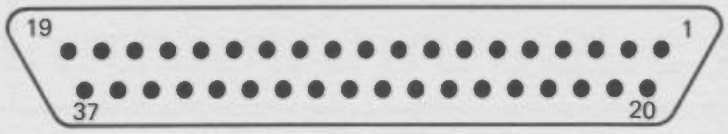


Figure 3 Timing Relationships

The single channel interface inputs and outputs (other than clocks) are routed through a rear panel 37-way D-type connector. Pin connection details are given in Figure 4. Open collector drivers and schmitt trigger receivers were chosen to allow low impedance twisted pair connections between the PMA and the codec digital interface. The PMA interface should therefore be mirrored externally in the digital interface to ensure correct operation. The clocks are connected separately via BNC, Siemens or WECO connectors, depending on choice of PMA option.

PIN NUMBER	SIGNAL
1 to 19	Ground
20	I/P DATA BIT 1
21	I/P DATA BIT 2
22	I/P DATA BIT 3
23	I/P DATA BIT 4
24	I/P DATA BIT 5
25	I/P DATA BIT 6
26	I/P DATA BIT 7
27	I/P DATA BIT 8 (Serial I/P)
28	I/P DATA VALID
29	O/P DATA BIT 1
30	O/P DATA BIT 2
31	O/P DATA BIT 3
32	O/P DATA BIT 4
33	O/P DATA BIT 5
34	O/P DATA BIT 6
35	O/P DATA BIT 7
36	O/P DATA BIT 8 (Serial O/P)
37	O/P DATA VALID



Viewed from rear of instrument

Figure 4 Single Channel Interface Connector

Making A-A, A-D and D-A Measurements

To construct a sequence of measurements to be performed on a codec, the PMA is programmed in the normal way with the number of channels in the SYSTEM PARAMETERS display set to one. Of course, measurements like crosstalk or frame alignment (3779A only) are now meaningless and should not be entered in a sequence.

It should be noted, however, that there is no automatic digital looping facility within the PMA when using the single channel interface. Thus A-A, A-D and D-A measurements cannot be mixed and run sequentially within a sequence in the same way as for serial PCM operation at 2048 kb/s or 1544 kb/s. There is a way round this problem by using "dummy" D-A idle channel noise measurements which generate 8-bit digital code words that can be detected by the external interface circuit between the PMA and the codec. These code words are used to loop and unloop the digital side of the codec as desired.

```
                SYSTEM PARAMETERS
================================================
CHANNEL PARAMETERS *   :*
SEQUENCE NUMBER:          1
No OF CHANNELS:           1
1kHz REF OUTPUT (Vrms): 3.535
BACKGROUND PCM  (D-A) : 1
 (1=as generated 2=as received)

                TEST LABELS
------------------------------------------------
    15        10      1979         0
     0         0         0         0
  3779         0      2631      2911

* use "ENTER" key to access

**********A-A*****STOP**********
```

Figure 5 3779 PMA System Parameters Display

The following arrangement is an example of how digital looping on a codec can be implemented as part of the external interface circuit. An 8-bit code word programmed as a code level between 0 and +127 or −127 in a dummy D-A ICN measurement is detected by two 4-bit comparators. The presence of the word for several frames is detected by a counter to ensure single occurrences of the code word in other D-A measurements do not trigger the looping or unlooping function. The outputs from the comparators and counter are then gated to produce a "loop" or "unloop" logic signal which in turn can drive whatever looping circuit is most convenient to the user.

When the output of the PMA consists of 8-bit code (xy_1) for a number of consecutive frames, then LOOP for A-A measurements is achieved.

When the output of the PMA consists of 8-bit code (xy_2) for a number of consecutive frames, then UNLOOP for A-D and D-A measurements is achieved.

It is advisable to use codes above ±118 which are not often encountered over a number of consecutive frames in other D-A measurements.

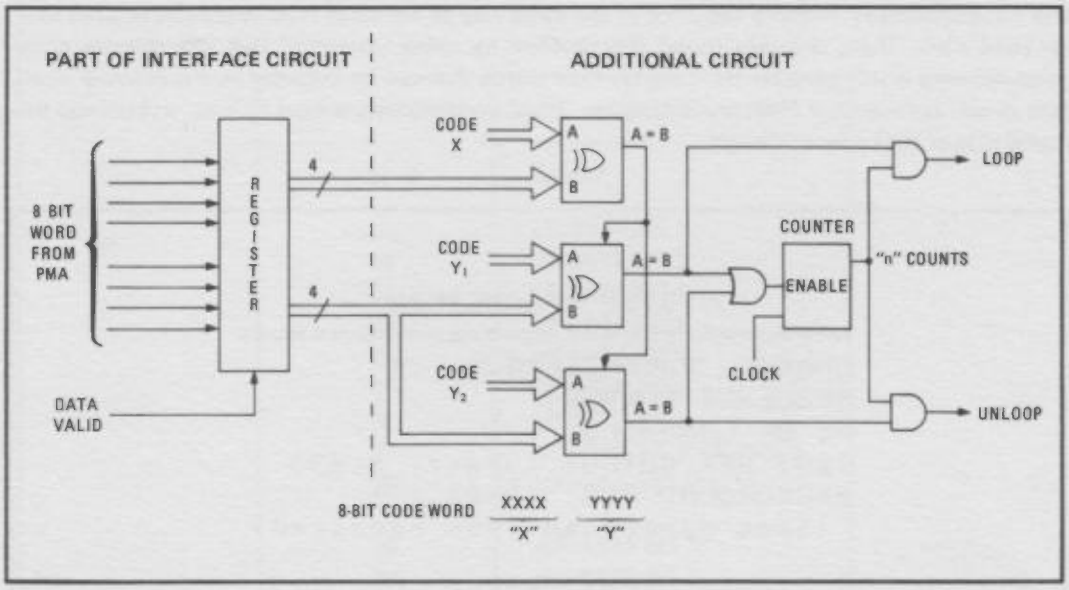


Figure 6 Block Diagram for Digital Looping Circuit

Driving an IC Handler & Indicating Failed Measurements

The same principle outlined in the previous section using dummy D-A ICN measurements can also be used to drive an integrated circuit device handler and "binning" system. For example, a specific code as a dummy measurement at the end of a test sequence can be used to index the handler to the next device. This idea can be extended to a family of dummy measurements each having a code identifying the measurement within the sequence which was failed by the device under test. The GO TO statement in the IF FAIL column of the sequence can be used to make the PMA jump to a particular dummy measurement thus exiting from the test sequence and indicating the type of failure.

With this approach, it can be seen that the PMA does not require an external controller to realise a measuring system which includes a device handler and sorter, provided some simple external logic circuitry can be designed and constructed.

```
          SEQ 1    !IF PASS!IF FAIL
==========================================
 1*ICN PSOPH D-A!         !
 2!GAIN      A-A!         !     >18
 3!GvL-noise A-A!         !     >19
 4!GvL-tone  A-A!         !     >19
 5!ICN PSOPH A-A!         !     >20
 6!QD -noise A-A!         !     >19
 7!ICN PSOPH D-A!         !
 8!GAIN      A-D!         !     >21
 9!GAIN -Pc  A-D!         !     >21
10!GvL-tone  A-D!         !     >22
11!ICN PSOPH A-D!         !     >23
12!PEDESTAL  A-D!         !     >23
13!GAIN      D-A!         !     >24
14!GvL-tone  D-A!         !     >25
15!QD -tone  D-A!         !     >25
16!ICN PSOPH D-A!         !     >26
17!ICN PSOPH D-A!      > 1!     > 1
##########D-A######STOP##########
```

Figure 7 Measurement Sequence with Dummy D-A Measurements

Applications

The PMA approach to single channel PCM codec testing is a relatively low-cost solution when compared with large computer-based systems normally used for integrated circuit testing. Its ease of programming and use mean there are no hidden software costs in getting a system running. The PMA provides an ideal quality assurance or incoming inspection test system for assessment of codecs.

For production testing, either at wafer probe or packaged device levels, a single PMA is rather slow compared with a high cost dedicated test system. However, the required throughput can be achieved at comparable or lower cost by running several PMA test stations in parallel. This has the added advantage of spreading the risk of breakdown and loss of throughput that would occur with a single high cost test system.

It's perhaps worth noting that transmission measurements of any significant accuracy cannot be done in times similar to the tests performed on straightforward analog or digital IC devices. The actual test time for each device will of course depend on the number and type of measurements within the test sequence and the number of points within each measurement. The PMA itself has two basic running speeds. Running a test sequence in the SEQUENCE DISPLAY mode is much faster than in RESULT DISPLAY since the instrument doesn't have to wait to indicate measured results on the CRT for an operator to read.

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For more information:
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