Early GaAs IC Recollections Rory Van Tuyl March 2024

1979-1981 saw the first chapter in the long history of III-V IC development in Santa Rosa. I led this team, reporting to section manager Pat Wang under R&D manager Doug Gray. Tech Center was initially managed by George Bodway during this period. Later, George moved on and was replaced by Byron Anderson

We transferred this process to Production in 1981 and reported on it in this publication:

"A Manufacturing Process for Analog and Digital Gallium Arsenide Integrated Circuits" IEEE Transactions on Electron Devices (Volume: 29, Issue: 7, July 1982)

Key attributes of this process were:

• Semi-insulating GaAs free from Cr doping (LEC could be grown with a natural deeplevel acceptor called EL2);

- At long last: Round Wafers!
- Silicon ion implantation directly into bulk material, obviating the need for an epitaxial buffer layer;
- Low pressure chemical-vapor-deposited [LPCVD] implant anneal cap that remained in place as a field oxide for metal lift assist;
- Proton isolation of conductive areas to replace mesa isolation, reduce sidegating and ensure planarity;
- Silicon nitride deposited by plasma-enhanced CVD to passivate the MESFETs and double as a dielectric film for capacitors;
- Reliable metallization [Mo-Au and Cr-Pt-Au] to replace the Cr-Au used in the research phase;
- Spun-on polyimide intermetal dielectric to support, isolate and overcoat the second metal;
- In-process control of MESFET Idss to within 10%;
- Semi-automated post-process testing with high frequency wafer probes.

This process formed the basis for future, higher-performance technologies developed at Tech Center after I moved on in 1984. The MMIC process, optimized for microwave, followed a few years later and supported robust frequency coverage to 26.5 GHz. The subsequent MODIC process (a.k.a. PH9) pushed active device frequency coverage to 50 GHz.

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